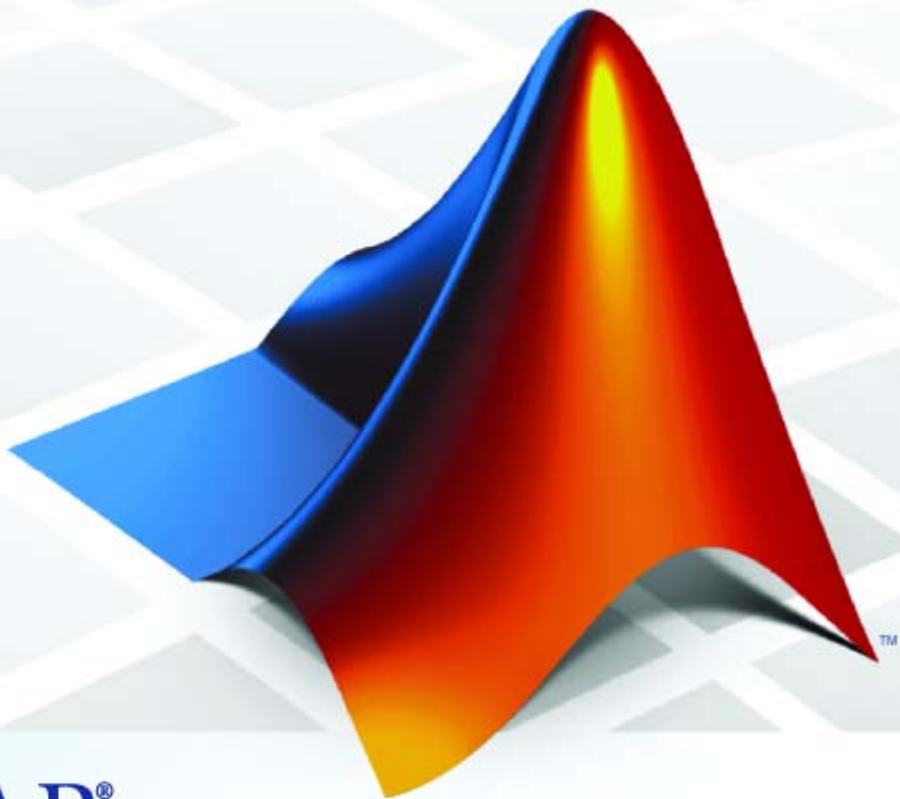


Simulink® Design Verifier™ 1

User's Guide



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508-647-7001 (Fax)



The MathWorks, Inc.
3 Apple Hill Drive
Natick, MA 01760-2098

For contact information about worldwide offices, see the MathWorks Web site.

Simulink® Design Verifier™ User's Guide

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March 2008	Online only	Revised for Version 1.2 (Release 2008a)
October 2008	Online only	Revised for Version 1.3 (Release 2008b)
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Acknowledgment

The Simulink® Design Verifier™ software uses Prover Plug-In® products from Prover® Technology to generate test cases and prove model properties.



Acknowledgment

Acknowledgment

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Product Overview

The Simulink Design Verifier software extends the Simulink® product by performing exhaustive formal analyses of your models to confirm that they behave correctly.

The Simulink Design Verifier software allows you to perform the following tasks:

- Generate test cases that achieve model coverage and custom objectives you specify in a model.
- Prove properties that you specify in a model, and identify examples of any property violations.
- Detect unreachable design elements in a model, such as inaccessible subsystems, illegal switch conditions, and unachievable states.
- Produce detailed reports regarding test case generation and property proofs.

Before You Begin

In this section...
“What You Need to Know” on page 1-3
“Required Products” on page 1-3

What You Need to Know

Getting started with the Simulink Design Verifier software requires that you have some experience using model coverage, as well as building and running Simulink models.

To learn more about these topics, see the following:

- “Using Model Coverage” in the *Simulink® Verification and Validation™ User’s Guide*
- *Simulink Getting Started Guide* and *Simulink User’s Guide*

Required Products

You must have the following products installed to use the Simulink Design Verifier software:

- MATLAB®
- Simulink
- Simulink Verification and Validation

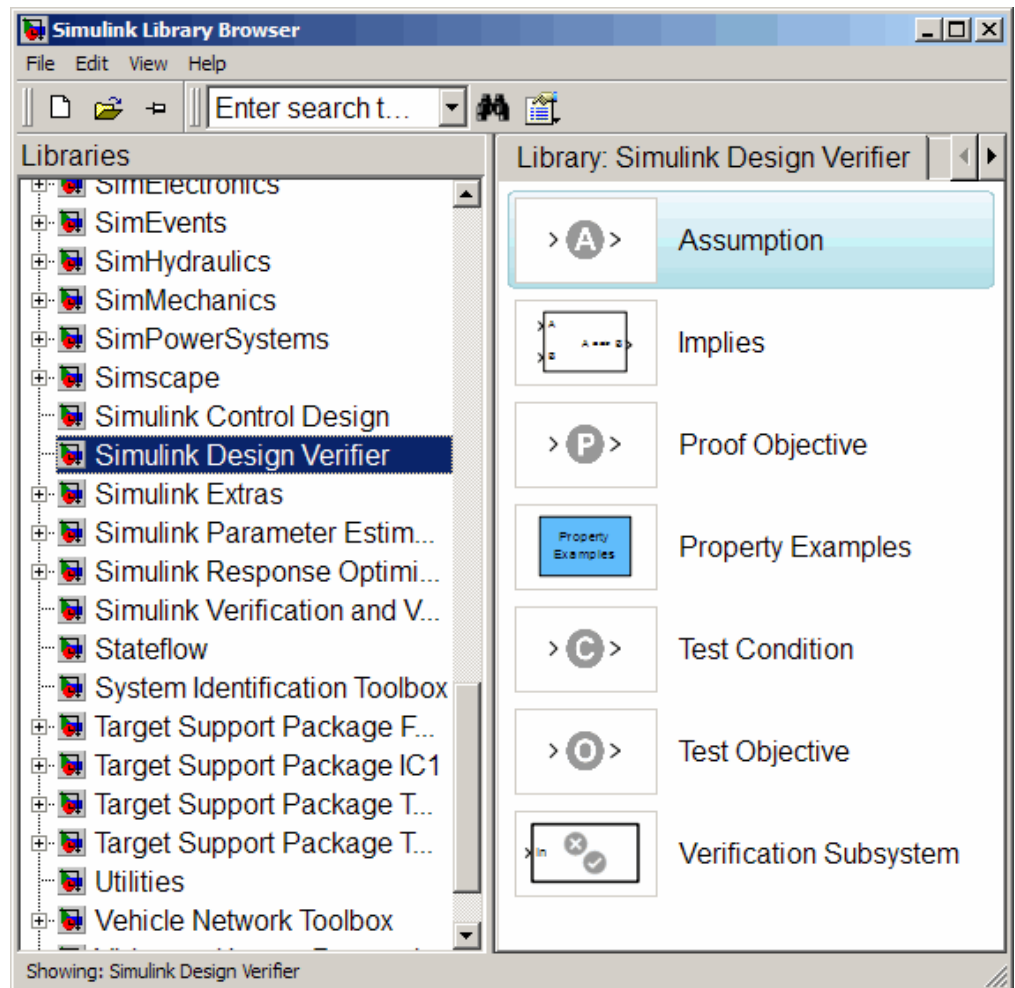
If you want to use the Simulink Design Verifier software with Stateflow® charts, you must have the following software product:

- Stateflow

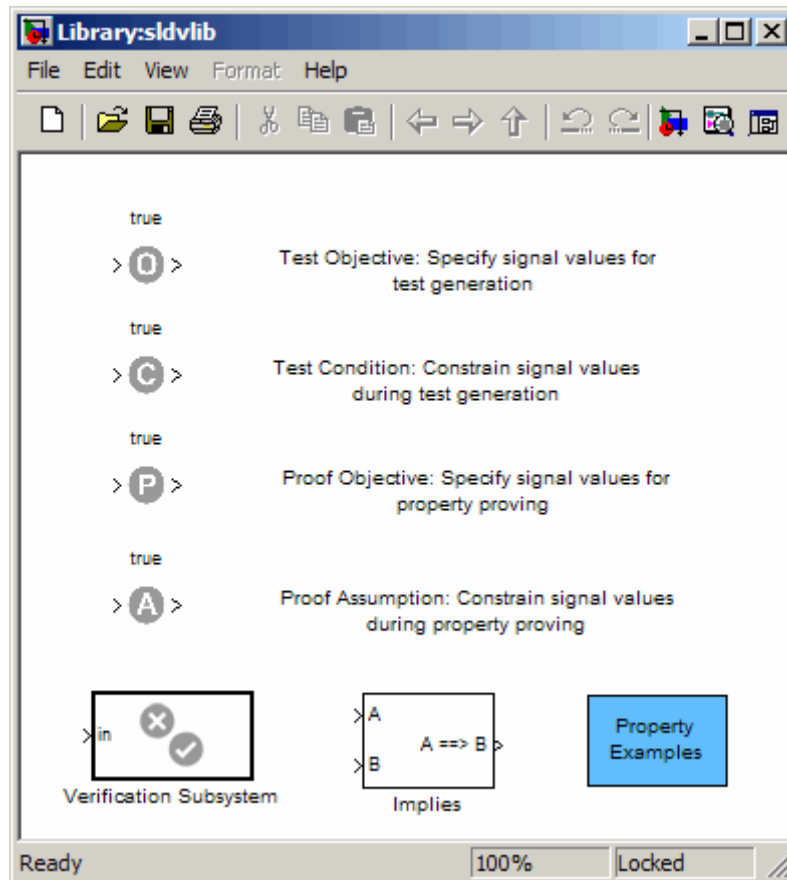
Starting the Simulink Design Verifier Software

The Simulink Design Verifier software is part of your MATLAB installation.

To open the Simulink Design Verifier block library, type `simulink` at the MATLAB prompt to display the Simulink Library Browser, and then select the **Simulink Design Verifier** entry in the contents tree.



Alternatively, type `sldvlib` at the MATLAB prompt to display the Simulink Design Verifier library.



Analyzing a Model

In this section...
“About This Demo” on page 1-6
“Opening the Model” on page 1-6
“Generating Test Cases” on page 1-7
“Combining Test Cases” on page 1-23

About This Demo

The following sections describe a demo model, Cruise Control Test Generation. This demo illustrates how to use the Simulink Design Verifier software to generate test cases that achieve complete model coverage. Through this demo, you learn how to analyze models with the Simulink Design Verifier software and interpret the results.

Opening the Model

To open the Cruise Control Test Generation model, enter `sldvdemo_cruise_control` at the MATLAB prompt.

The Cruise Control Test Generation model opens.

Simulink Design Verifier
Cruise Control Test Generation

This model is configured to generate test cases that achieve complete model coverage. By default Simulink Design Verifier generates test cases that satisfy objectives in the fewest steps. One of the test objectives forces the discrete integrator in the PI controller to exceed its upper limit. When you run Simulink Design Verifier without constraints the limit is exceeded in a single step by forcing speed to be 500. The constraint on speed limits the values in test cases between 0 and 100. This forces the test cases to take several samples to exceed the integrator limit.

Run (double-click)
Run Simulink Design Verifier

Toggle Speed Constraint (double-click)
Toggle Constraint

View Options (double-click)
View Simulink Design Verifier Options

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Ready 100% FixedStepDiscrete

Generating Test Cases

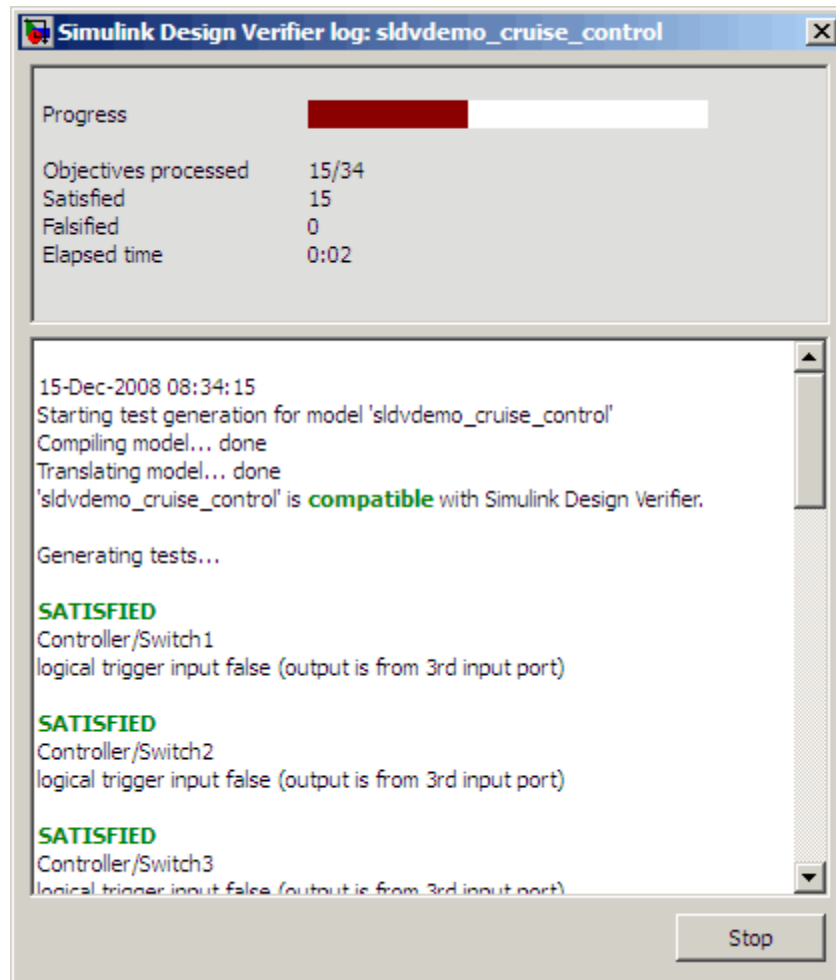
- “Running the Analysis” on page 1-8

- “Exploring the Test Harness” on page 1-10
- “Interpreting the Simulink® Design Verifier HTML Report” on page 1-15

Running the Analysis

To generate test cases for the Cruise Control Test Generation model, open the model window and double-click the block labeled **Run**.

The Simulink Design Verifier software begins analyzing the model to generate test cases. During its analysis, the software displays a log window.



The log window updates you on the progress of the Simulink Design Verifier software as it analyzes the model.

Note If you need to terminate an analysis while it is running, click **Stop**. The software asks you if you want to produce results. If you click **Yes**, the software creates the data file and report based on the results achieved so far. The names of those files appear in the log window.

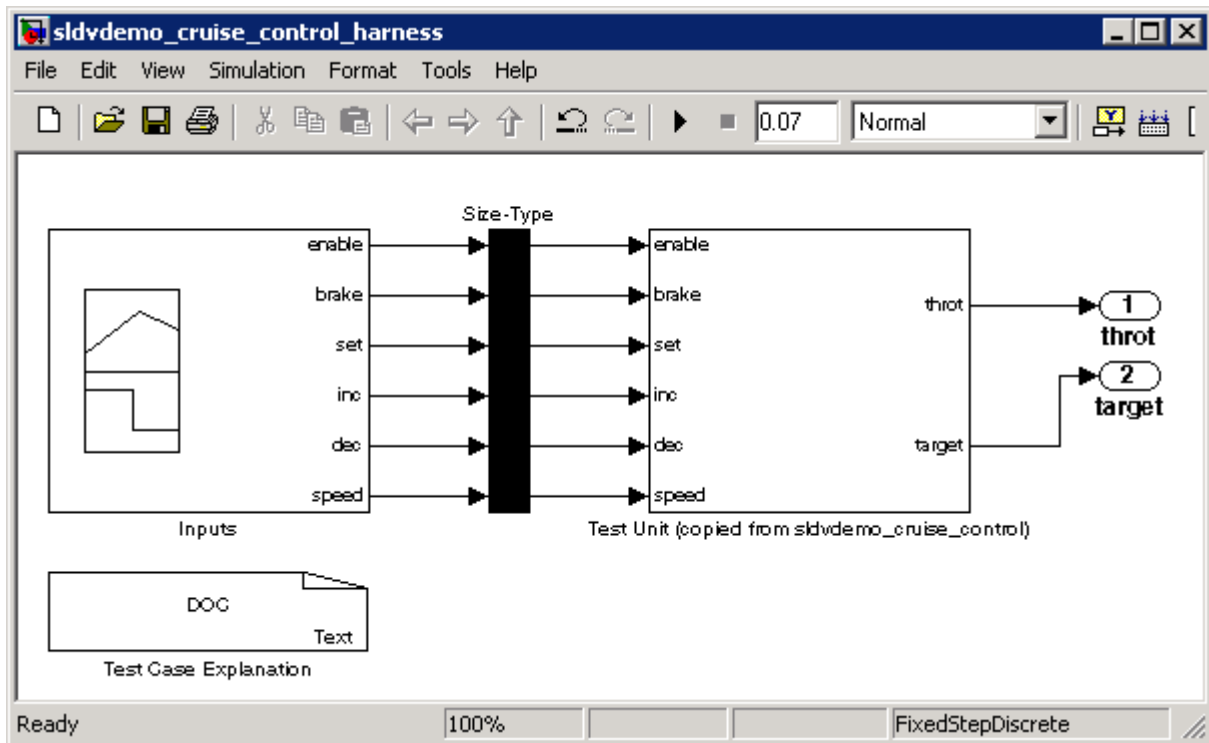
When the Simulink Design Verifier software completes its analysis, it opens:

- Test harness model: `sldvdemo_cruise_control_harness.mdl`
- Signal Builder dialog box containing the test-case signals
- HTML report containing the analysis results:
`sldvdemo_cruise_control_report.html`

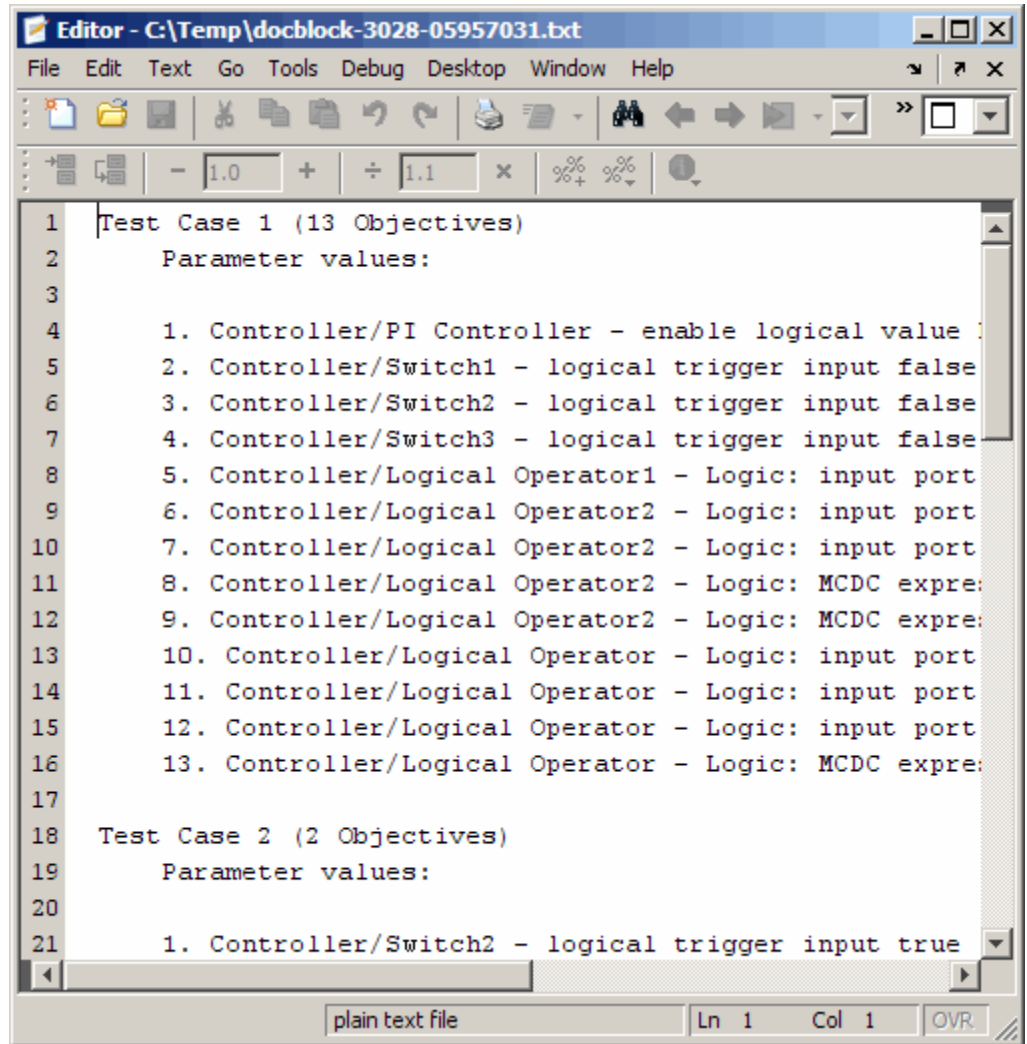
The sections that follow describe the test harness, the Signal Builder data, and the HTML report in detail.

Exploring the Test Harness


The Simulink Design Verifier software creates a test harness model when it completes its analysis. The test harness for the Cruise Control Test Generation model appears as shown in the following figure.

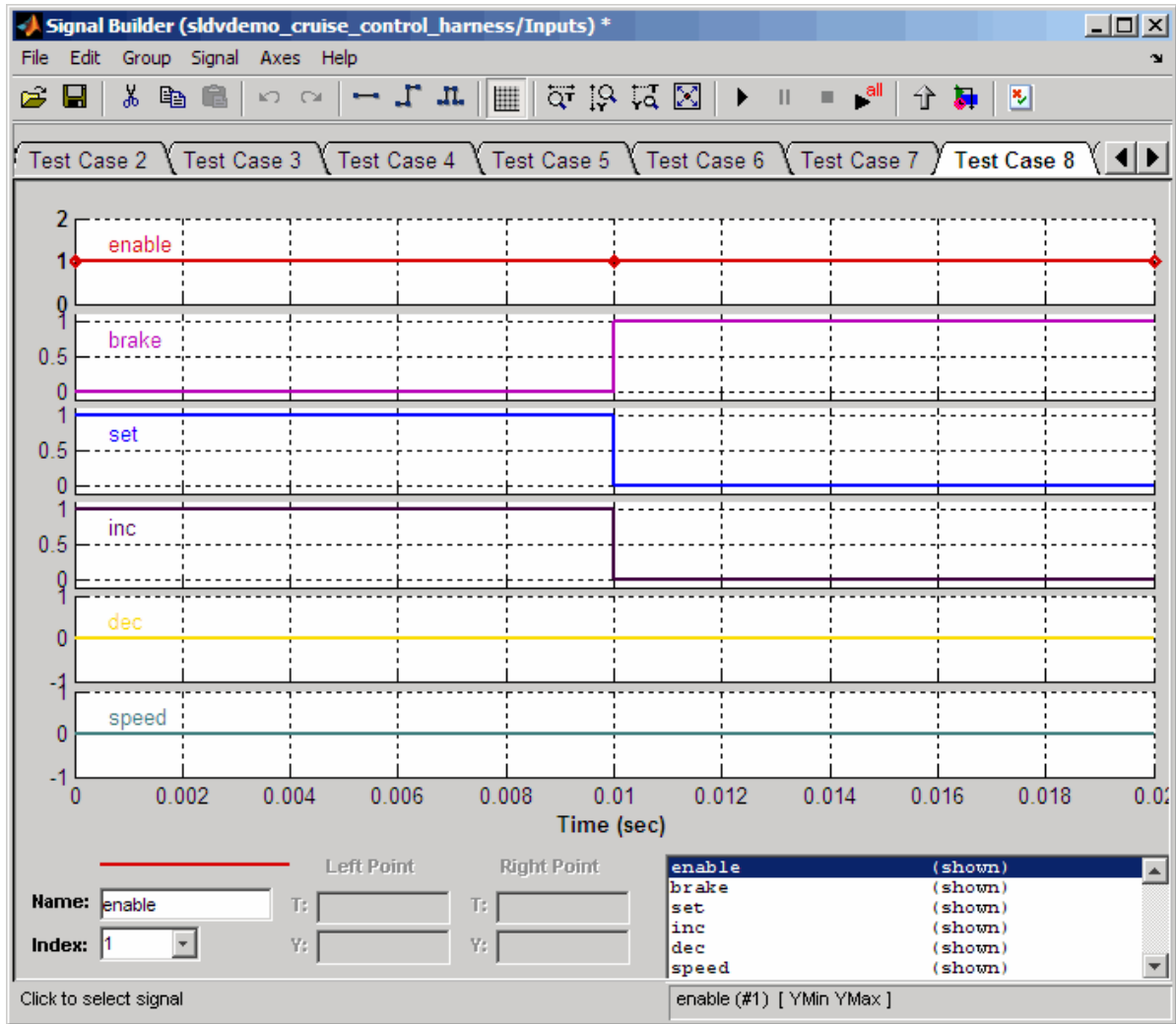


- 1 The block labeled Test Case Explanation is a DocBlock block that documents the generated test cases. Double-click the Test Case Explanation block to view a description of each test case in terms of the objectives that the test case satisfies.



- 2 The block labeled Test Unit is a Subsystem block that contains a copy of the original model the software analyzed. Double-click the Test Unit block to view its contents and confirm that it is a copy of the Cruise Control Test Generation model.

- 3** The block labeled Inputs is a Signal Builder block that contains the generated test case signals. Double-click the Inputs block to open the Signal Builder dialog box and view the 10 test case signals.
- 4** In the Signal Builder dialog box, click the right-facing arrow next to the test case tabs  to find the **Test Case 8** tab.
- 5** Click the **Test Case 8** tab to display the signal values for Test Case 8.




In Test Case 8 at 0.1 seconds:

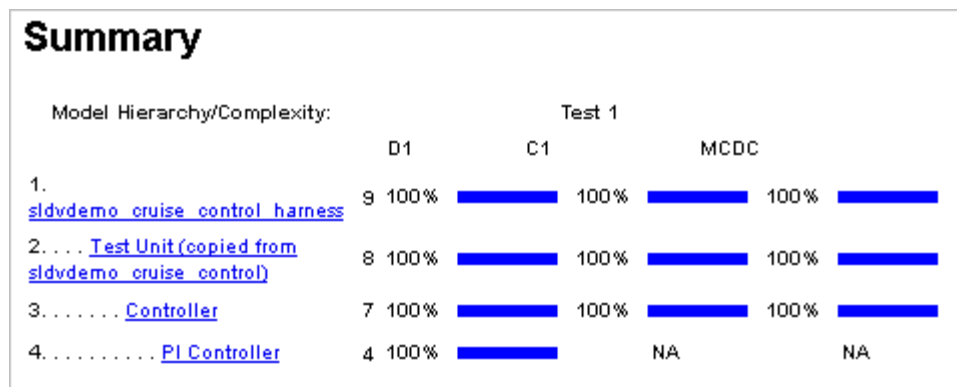
- The enable signal remains 1.
- The brake signal transitions from 0 to 1.
- The inc and set signals transition from 1 to 0.

- The dec and speed signals remain 0.

This group of signals achieves the test objectives described in the Test Case Explanation block.

- 6 To confirm that the Simulink Design Verifier software achieved complete model coverage, simulate the test harness using all the test cases. In the Signal Builder dialog box, click the **Run all** button .

The Simulink software simulates the test harness using all the test cases, while the Simulink Verification and Validation software collects model coverage information and displays a coverage report with the following summary.



The coverage report indicates the Simulink Design Verifier software generated test cases that achieve complete coverage for the Cruise Control Test Generation model.

Interpreting the Simulink Design Verifier HTML Report

The Simulink Design Verifier software creates an HTML report that summarizes its analysis results.

If the report is not open in a Web Browser window, open it now. The path name is:

```
matlabroot/sldv_output/sldvdemo_cruise_control/sldvdemo_cruise_control_report.html
```

Note The log window contains the exact path name for the HTML report.

The HTML report includes the following chapters.

Table of Contents
1. Summary
2. Analysis Information
3. Test Objectives Status
4. Model Items
5. Test Cases

Each the following sections for a description of each report chapter:

- “Summary” on page 1-16
- “Analysis Information” on page 1-17
- “Test Objectives Status” on page 1-19
- “Model Items” on page 1-21
- “Test Cases” on page 1-22

Summary. In the **Table of Contents**, click **Summary** to display the Summary chapter, which includes the following information:

- Name of the model
- Mode of the analysis (test generation or property proving)
- Status of the analysis
- Number of objectives satisfied

Chapter 1. Summary

Analysis Information

Model: sldvdemo_cruise_control
Mode: TestGeneration
Status: Completed normally

Objectives Status

Number of Objectives: 34

Objectives Satisfied: 34

Analysis Information. In the **Table of Contents**, click **Analysis Information** to display information about the analyzed model and the analysis options.

Chapter 2. Analysis Information

Table of Contents

[Model Information](#)
[Analysis Options](#)
[Constraints](#)
[Approximations](#)

Model Information

File: \\mathworks\ah\devel\jobarchive\Aslrv\latest_pass\matlab\toolbox\slv\slvdemos\slvde
 Version: 1.49
 Time: Thu Nov 20 22:52:48 2008
 Stamp:
 Author:

Analysis Options

Mode: TestGeneration
 Test Suite Optimization: CombinedObjectives
 Maximum Testcase Steps: 500 time steps
 Test Conditions: UseLocalSettings
 Test Objectives: UseLocalSettings
 Model Coverage Objectives: MCDC
 Maximum Processing Time: 60s
 Block Replacement: off
 Parameters Analysis: on
 Parameters Configuration File: slv_params_template.m
 Save Data: on
 Save Harness: on
 Save Report: on

Constraints

Name	Constraint
constraint	[0, 100]

Approximations

Simulink Design Verifier performed the following approximations during analysis. These can impact the precision of the results generated by Simulink Design Verifier. Please see the product documentation for further details.

 	Type	Description
1	Rational approximation	The model includes floating-point arithmetic. Simulink Design Verifier approximates floating-point arithmetic with rational number arithmetic.

Test Objectives Status. In the **Table of Contents**, click **Test Objectives Status** to display a table of satisfied objectives. The following figure shows a partial list of the objectives satisfied in the Cruise Control Test Generation model.

Chapter 3. Test Objectives Status

Table of Contents

[Objectives Satisfied](#)

Objectives Satisfied

Simulink Design Verifier found test cases that exercise these test objectives.

#:	Type	Model Item	Description	Test Case
1	Decision	Controller/PI Controller	enable logical value F	1
2	Decision	Controller/PI Controller	enable logical value T	5
3	Decision	Controller/Switch1	logical trigger input false (output is from 3rd input port)	1
4	Decision	Controller/Switch1	logical trigger input true (output is from 1st input port)	5
5	Decision	Controller/PI Controller/Discrete-Time Integrator	integration result <= lower limit F	5
6	Decision	Controller/PI Controller/Discrete-Time Integrator	integration result <= lower limit T	10
7	Decision	Controller/PI Controller/Discrete-Time Integrator	integration result >= upper limit F	5

The Objectives Satisfied table lists the following information for the model:

- **#** — Objective number.
- **Type** — Objective type.
- **Model Item** — Element in the model for which the objective was tested. Click this link to display the model with this element highlighted.
- **Description** — Description of the objective.
- **Test case** — Test case that achieves the objective. Click this link to get more information about that test case.

In the row for objective 17, click the test case number (8) to display more information about test case 8 in the report's Test Cases chapter.

Test Case 8

Summary

Length: 0.01 Seconds (2 sample periods)

Objective Count: 2

Objectives

Step	Time	Model Item	Objectives
2	0.01	Controller/Logical Operator2 Controller/Logical Operator2	Logic: input port 2 T Logic: MCDC expression for output with input port 2 T

Generated Input Data

Time	00.01
Step	12
enable	11
brake	01
set	10
inc	1-
dec	0-
speed	00

In this example, Test Case 8 satisfies 2 model coverage objectives. The following signal values achieve the objectives listed in the **Objectives** column of the table:

- The enable signal remains 1.
- The brake signal transitions from 0 to 1 at 0.1 seconds.

- The inc and set signals transition from 1 to 0 at 0.1 seconds.
- The dec and speed signals remain 0.

This information matches what you see in the test harness model. Specifically, the Inputs block in the test harness depicts identical signal values for Test Case 8, and the Test Case Explanation block lists 2 objectives that Test Case 8 achieves (see “Exploring the Test Harness” on page 1-10).

Model Items. In the **Table of Contents**, click **Model Items** to see detailed information about each item in the model that defines coverage objectives. This table includes the status of the objective at the end of the analysis. Click the links in the table to get detailed information about the satisfied objectives.

Chapter 4. Model Items

Table of Contents

[Controller/PI Controller](#)
[Controller/Switch1](#)
[Controller/PI Controller/Discrete-Time Integrator](#)
[Controller/Switch2](#)
[Controller/Switch3](#)
[Controller/Logical Operator1](#)
[Controller/Logical Operator2](#)
[Controller/Logical Operator](#)

This section presents, for each object in the model defining coverage objectives, the list of objectives and their individual status at the end of the analysis. It should match the coverage report obtained from running the generated test suite on the model, either from the harness model or by using the `sldvruntests` command.

Controller/PI Controller

[View](#)

#:	Type	Description	Status	Test Case
1	Decision	enable logical value F	Satisfied	1
2	Decision	enable logical value T	Satisfied	5

Controller/Switch1

[View](#)

#:	Type	Description	Status	Test Case
3	Decision	logical trigger input false (output is from 3rd input port)	Satisfied	1
4	Decision	logical trigger input true (output is from 1st input port)	Satisfied	5

Test Cases. In the **Table of Contents**, click **Test Cases** to display detailed information about each generated test case, including:

- Length of time to execute the test case
- Number of objectives satisfied

- Detailed information about the satisfied objectives
- Input data

See the section for Test Case 8 in “Test Objectives Status” on page 1-19

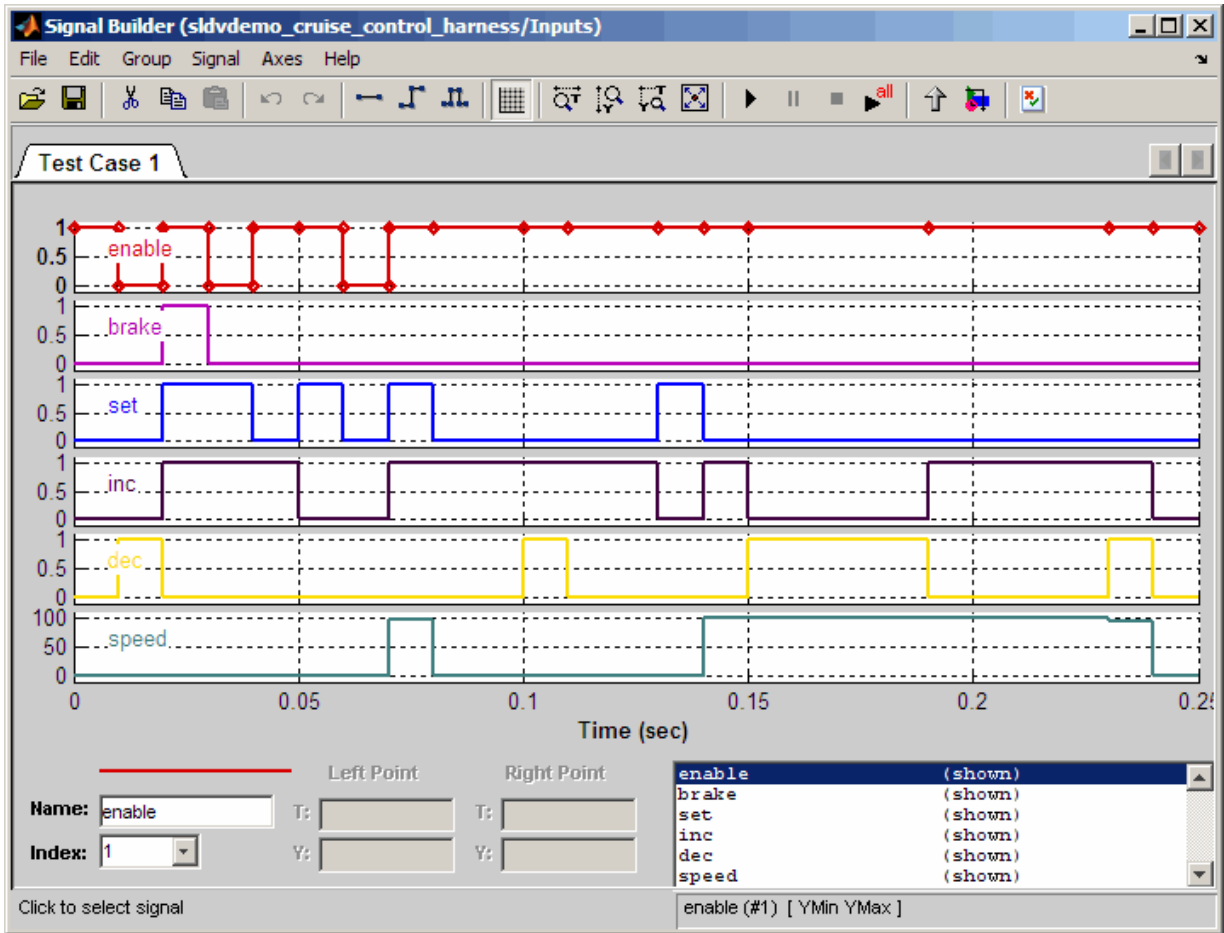
Combining Test Cases

If you prefer to review results that are combined into a smaller number of test cases, set the **Test suite optimization** parameter to **Long test cases**. When you use the **Long test cases** optimization, the analysis generates fewer, but longer, test cases that each satisfy multiple test objectives. This optimization creates a more efficient analysis and easier-to-review results.

Open the `sldvdemo_cruise_control` model and rerun the analysis with the **Long test cases** optimization:

- 1** Select **Tools > Design Verifier > Options**.
- 2** In the **Select** tree on the left side of the Configuration Parameters dialog box, in the **Design Verifier** category, select **Test Generation**.
- 3** Set the **Test suite optimization** parameter to **Long test cases**.
- 4** Click **Apply** and **OK** to close the Configuration Parameters dialog box.
- 5** In the `sldvdemo_cruise_control` model, double-click the block labeled **Run**.

The Signal Builder dialog box now contains one test case instead of ten test cases.



This HTML report contains one section describing Test Case 1.

Test Case 1

Summary

Length: 0.24 Seconds (25 sample periods)

Objective Count: 34

Objectives

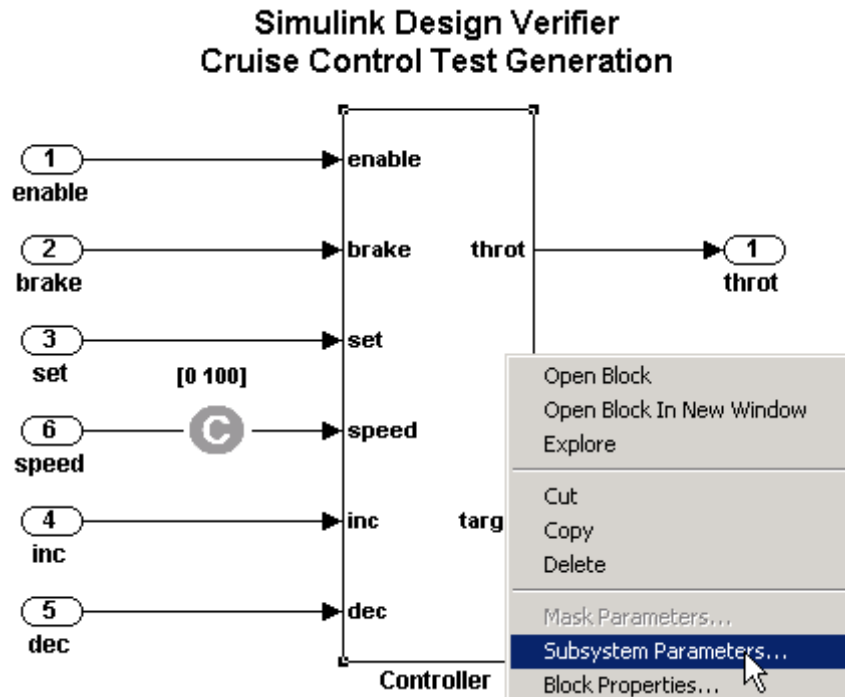
Step	Time	Model Item	Objectives
1	0	Controller/Switch2 Controller/Switch1 Controller/Switch3 Controller/Logical Operator Controller/Logical Operator1 Controller/Logical Operator2 Controller/Logical Operator2 Controller/PI Controller Controller/Logical Operator Controller/Logical Operator Controller/Logical Operator Controller/Logical Operator2 Controller/Logical Operator2	logical trigger input false (output is from 3rd input port) logical trigger input false (output is from 3rd input port) logical trigger input false (output is from 3rd input port) Logic: MCDC expression for output with input port 3 F Logic: input port 1 F Logic: MCDC expression for output with input port 2 F Logic: MCDC expression for output with input port 1 F enable logical value F Logic: input port 3 F Logic: input port 2 T Logic: input port 1 T Logic: input port 2 F Logic: input port 1 F
2	0.01	Controller/Switch3 Controller/Logical Operator	logical trigger input true (output is from 1st input port) Logic: input port 1 F
3	0.02	Controller/Switch1 Controller/Logical Operator Controller/Logical Operator2 Controller/Logical Operator Controller/Logical Operator2 Controller/Logical Operator1	logical trigger input true (output is from 1st input port) Logic: MCDC expression for output with input port 2 F Logic: MCDC expression for output with input port 1 T Logic: input port 2 F Logic: input port 1 T Logic: input port 1 T
4	0.03	Controller/Logical Operator	Logic: MCDC expression for output with input port 1 F

Analyzing a Subsystem

In addition to analyzing a model, you can analyze a subsystem within a model. This technique is good for large models, where you want to review the analysis in smaller, manageable reports.

This example analyzes the Controller subsystem in the `sldvdemo_cruise_control` model from “Analyzing a Model” on page 1-6.

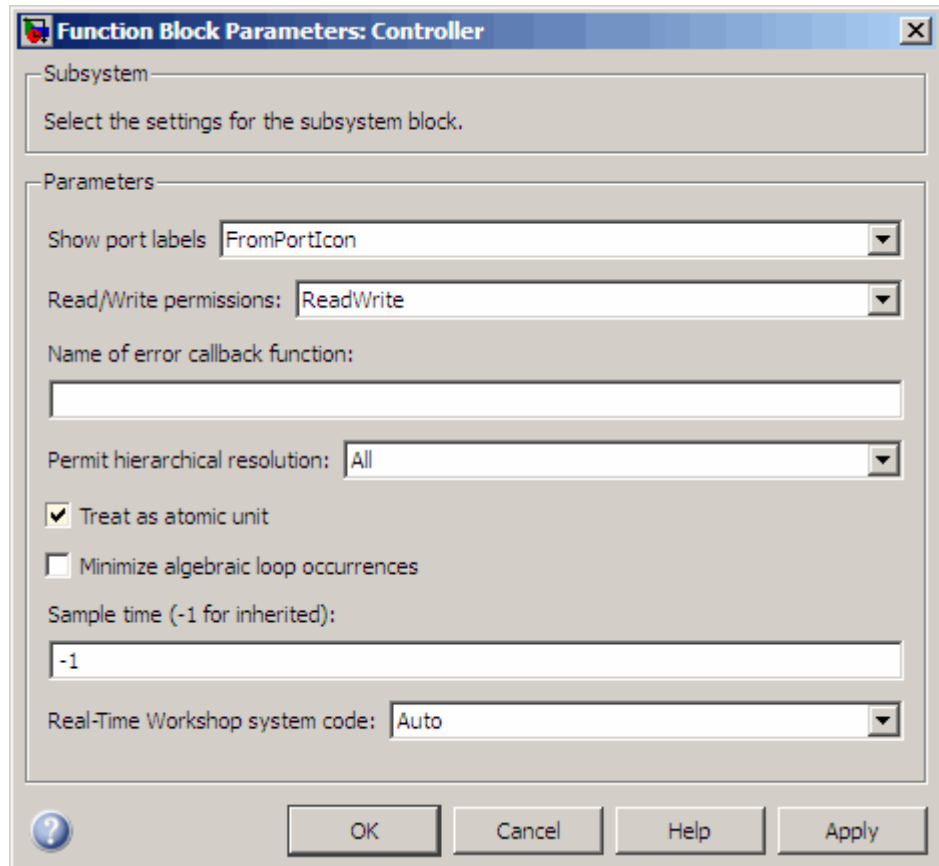
- 1 Enter `sldvdemo_cruise_control` at the MATLAB command line to open the Cruise Control Test Generation model.
- 2 Right-click the Controller subsystem, and select **Subsystem Parameters**.



- 3 In the Function Block Parameters dialog box, select **Treat as atomic unit**.

An *atomic subsystem* executes as a unit relative to the parent model; subsystem block execution does not interleave with parent block execution. This makes it possible to extract subsystems for use as standalone models.

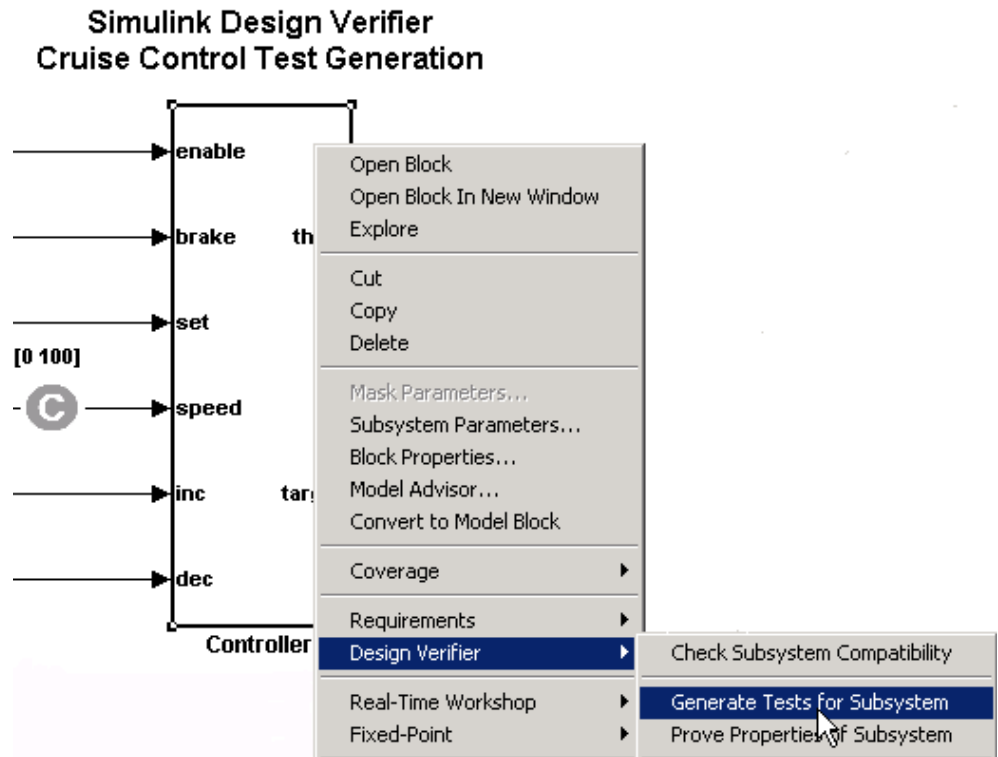
You must set the **Treat as atomic unit** parameter to analyze a subsystem with the Simulink Design Verifier software.



After you set the parameter, other options become available, but you can ignore them.

- 4 Click **Apply** and **OK** to close the dialog box.

- 5 Select **File > Save As** and save the Cruise Control Test Generation model under a new name.
- 6 To start the subsystem analysis and generate test cases, right-click the Controller subsystem, and select **Design Verifier > Generate Tests for Subsystem**.



- 7 The Simulink Design Verifier software creates and opens the following output. Except for the new model, all of these correspond to the model analysis output:
 - A new model containing just the Controller subsystem: `Controller.mdl`
 - Test harness model: `Controller_harness.mdl`
 - Signal Builder dialog box containing the test-case signals

- HTML report containing the analysis results: `Controller_report.htm`
- 8** Review the results of the subsystem analysis (harness model and HTML report) and compare them to the results of the full-model analysis described in “Analyzing a Model” on page 1-6.
- The subsystem analysis analyzes the Controller as a standalone model.
 - The Controller subsystem contains all the test objectives in the Cruise Control Test Generation model, so both analyses generate the same test cases.

Basic Workflow for Using the Simulink Design Verifier Software

The *Simulink Design Verifier User's Guide* is organized on the basis of workflow that you follow when generating tests for your model or proving its properties. This workflow is described in the following steps, which cite locations in the documentation that you can refer to for more information:

Step	Action	See...
1	Check the compatibility of your model.	Chapter 3, “Ensuring Compatibility with the Simulink® Design Verifier Software”
2	Optionally, prepare your model for analysis.	Chapter 4, “Working with Block Replacements” Chapter 5, “Specifying Parameter Configurations”
3	Set Simulink Design Verifier options.	Chapter 6, “Configuring Simulink® Design Verifier Options”
4	Generate test cases for your model or prove its properties.	Chapter 7, “Generating Test Cases” Chapter 8, “Proving Properties of a Model”
5	Interpret the results.	Chapter 9, “Reviewing the Results”

Learning More


In this section...
“Next Step” on page 1-31
“Product Help” on page 1-31
“The MathWorks Online” on page 1-32

Next Step

To begin learning how to use the Simulink Design Verifier software, see Chapter 3, “Ensuring Compatibility with the Simulink® Design Verifier Software”. Also see the following topics to continue your exploration of the software:

For...	See...
Exercise that walks you through the process of generating test cases for a model	“Generating Test Cases for a Model” on page 7-4
Exercise that walks you through the process of proving a model property	“Proving Properties in a Model” on page 8-4

Product Help

More information is available with your product installation. In the MATLAB desktop, click  for help, and then click the product name in the **Contents** pane.

For...	See...
List of blocks	Blocks — Alphabetical List
Tutorials	Examples in Documentation
More product demonstrations	Simulink Design Verifier Demos
What’s new in this product	Release Notes

The MathWorks Online

Point your Internet browser to the MathWorks Web site for additional information and support at

<http://www.mathworks.com/products/slidesignverifier/>

How the Simulink Design Verifier Software Works

- “Model Analysis with Simulink® Design Verifier Software” on page 2-2
- “Analyzing a Simple Model” on page 2-3
- “Analyzing Large Models” on page 2-5
- “Handling Incompatibilities with Automatic Stubbing” on page 2-6
- “Approximations” on page 2-14

Model Analysis with Simulink Design Verifier Software

Simulink Design Verifier software is an efficient analysis tool that explores the simulation behavior of a model. It searches the possible values of model inputs and block parameters to find a simulation that satisfies test objectives. The software also proves model properties and generates examples of violations.

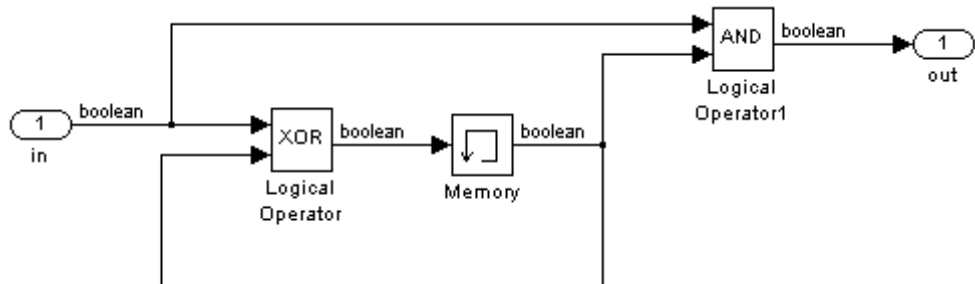
Such analysis always begins with the initial configuration of the model and can span an arbitrary number of time steps. Generally, there is an infinite number of paths through the model because the values of inputs are independent from one time step to the next, and there is no fixed limit to the number of time steps.

If the software finds no way to reduce the search space, it would continue its analysis indefinitely. Thus, the software limits the analysis by tracking the persistent information in the model such as discrete states, data-store memories, and persistent variables.

After an analysis explores all possible inputs and parameters from all possible configurations, the results equal those of a complete search of every possible infinite sequence of inputs parameters.

Analyzing a Simple Model

This simple Simulink model includes two Logical Operator blocks and a Memory block.



The persistent information in this model is limited to the Boolean value of the Memory block. The input to the model is a single Boolean value. The following table describes the complete behavior of the model, including the behavior that would result from an arbitrarily long sequence of inputs.

#	Input	Memory Value	Output of XOR Block = Next Memory Value	Output of AND Block
1	false	false	false	false
2	true	false	true	false
3	false	true	true	false
4	true	true	false	true

Suppose you want to generate test cases that result in a true output; this goal is your *test objective*. If you run the Simulink Design Verifier software to generate test cases that result in a true output, the software searches this table to see if such a scenario is possible.

After the Simulink Design Verifier software discovers a configuration that satisfies the test objective (in this case, when both the input and the Memory block output are true), it needs to find a path to reach this configuration from

the initial conditions. If the initial memory value is true, the test case only needs to be a single time step (row 4) where the input was true.

If the initial memory value is false (the default), the test case must force the memory value to be true. In this example, the path requires two steps:

- 1** The input value is true and the memory value is false (row 2). Thus, the output of the XOR block is true, making the memory value true.
- 2** Now that the input value and memory value are both true (row 4), the output is true, so the analysis achieves the specified test objective.

An infinite number of test cases can cause the output to be true, and regardless of the state value, the output can be held false for an arbitrary time before making it true. When the Simulink Design Verifier software searches, it returns the first test case it encounters that satisfies the objective. This case is invariably the simulation with the fewest time steps. Sometimes you may find this result undesirable because it is unrealistic or does not satisfy some other test requirement.

The same basic principles from this example apply to property proving and test case generation. During test case generation, option parameters explicitly specify the search criteria. For example, you can specify that Simulink Design Verifier software find paths for all outputs or find only those paths that make where the output is true.

During property proving, you specify a functional requirement, or property, that you want the Simulink Design Verifier software to prove, for example, that the output is always true. If the search completes without finding a path that violates the property, the proof of that property completes successfully. If the software finds a path where the output is false, it creates a counterexample that causes the output to be false.

Analyzing Large Models

In larger, more complicated models, the Simulink Design Verifier software uses mathematical techniques to simplify the analysis:

- It identifies portions of the model that do not affect the desired objectives.
- It discovers relationships within the model that reduce the complexity of the search.
- It reuses intermediate results from one objective to another.

In this way, the problem is reduced to a search through the logical values that describe your model.

For detailed information about analyzing large models, see Chapter 10, “Analyzing Large Models and Improving Performance”.

Handling Incompatibilities with Automatic Stubbing

In this section...
“What Is Automatic Stubbing?” on page 2-6
“Analyzing a Model Using Automatic Stubbing” on page 2-6

What Is Automatic Stubbing?

Automatic stubbing allows you to run a test case generation or property-proving analysis on a model that contains elements that the Simulink Design Verifier software does not support.

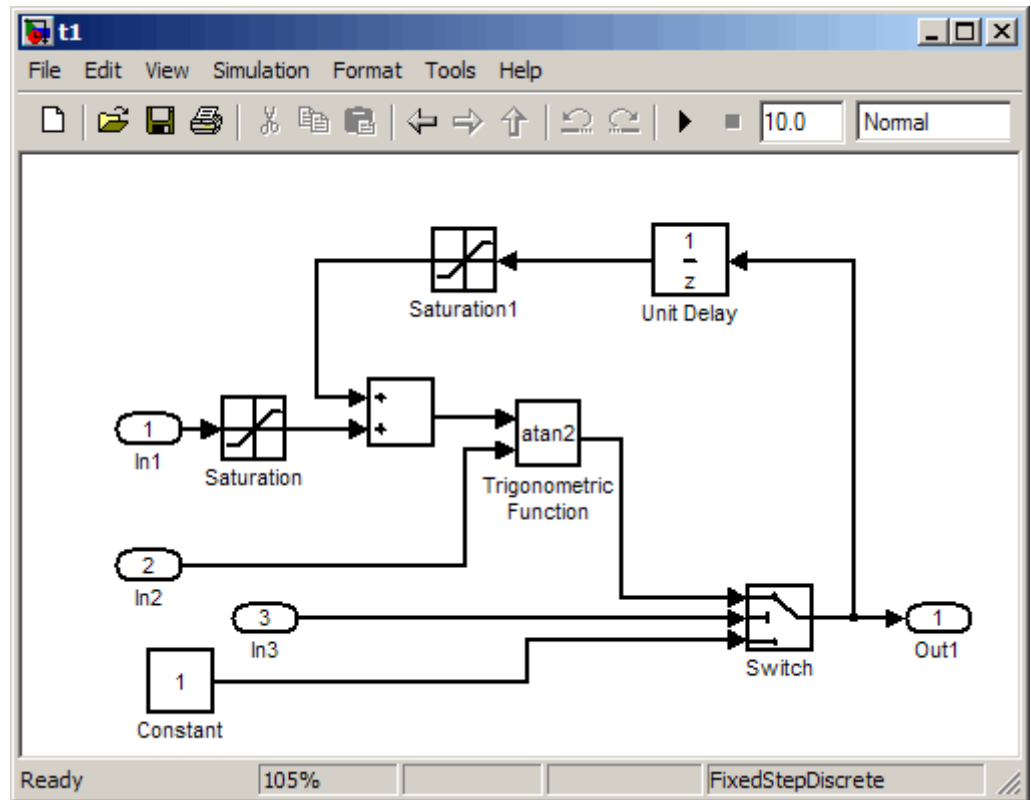
When you enable automatic stubbing option, the software considers only the interface of the unsupported elements, not their actual behavior. This technique allows the software to complete the analysis. However, the analysis may achieve only partial results if any of the unsupported model elements affect the simulation outcome.

Analyzing a Model Using Automatic Stubbing

This section describes a workflow for using automatic stubbing, using a simple Simulink model (t1) as an example.

- “Checking Model Compatibility” on page 2-7
- “Turning On Automatic Stubbing” on page 2-10
- “Reviewing the Results” on page 2-12
- “Achieving Complete Results” on page 2-13

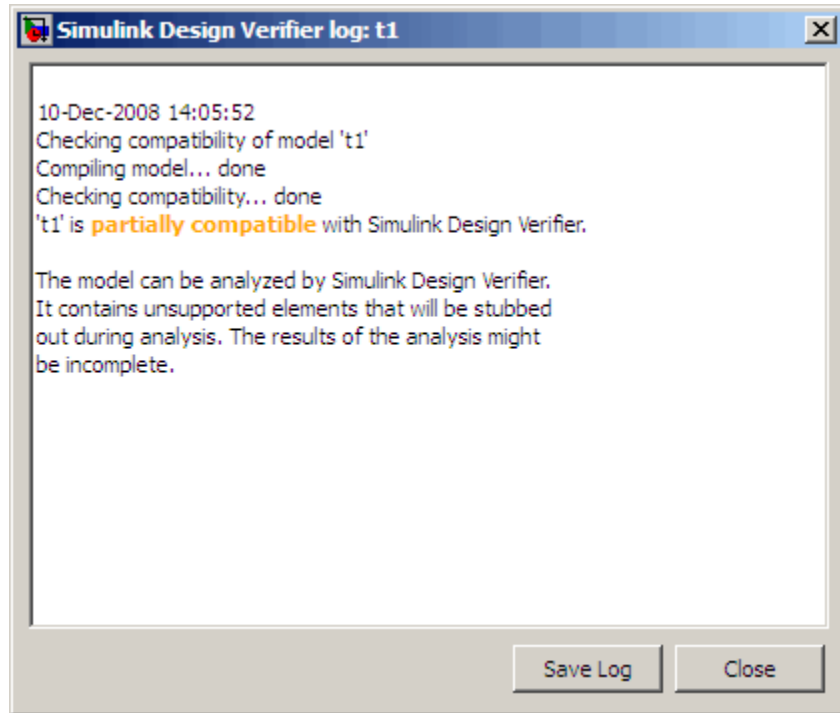
The t1 model contains a Trigonometric Function block, which is not compatible with the Simulink Design Verifier software.



Checking Model Compatibility

From the Model Editor, there are two ways to check whether a model is compatible with the Simulink Design Verifier software:

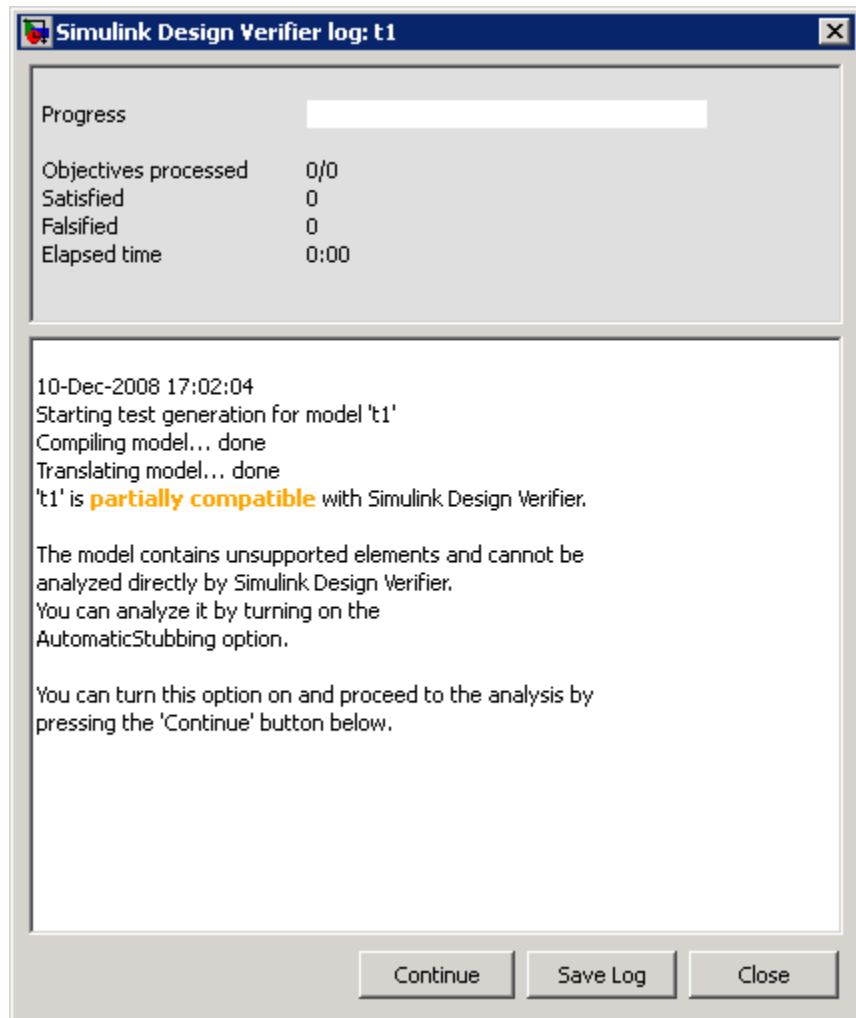
- Run the Simulink Design Verifier compatibility check by selecting **Tools > Design Verifier > Check Model Compatibility**.



- Select the analysis that you want:
 - **Tools > Design Verifier > Generate Tests**
 - **Tools > Design Verifier > Prove Properties**

The software first checks the compatibility of the model. If the model itself is incompatible, for example, if it uses a variable-step solver, the analysis cannot continue.

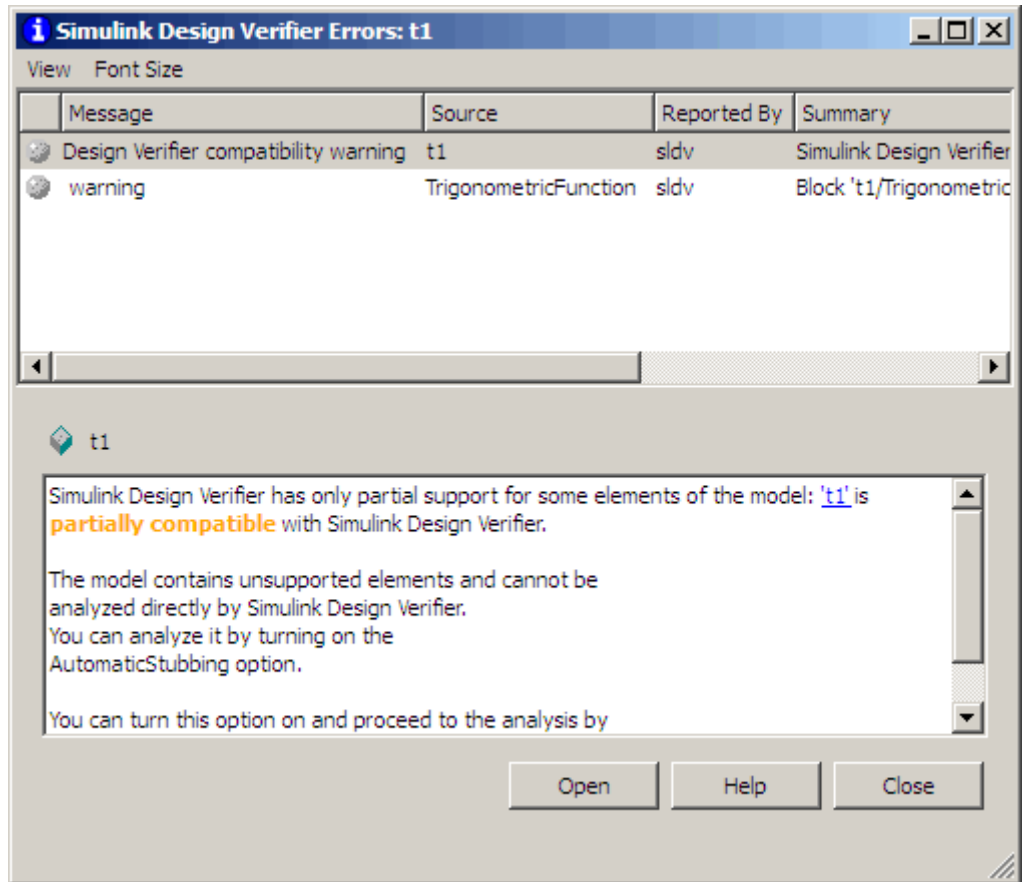
If it finds incompatible elements in the model, the software stops and asks if you want to turn on automatic stubbing.



You can:

- Save the log file.
- Continue the analysis.
- Terminate the analysis.

The Simulation Diagnostics Viewer is also displayed, listing the incompatibilities. (For more information about this dialog box, see “Simulation Diagnostics Viewer” in the *Simulink User’s Guide*.)

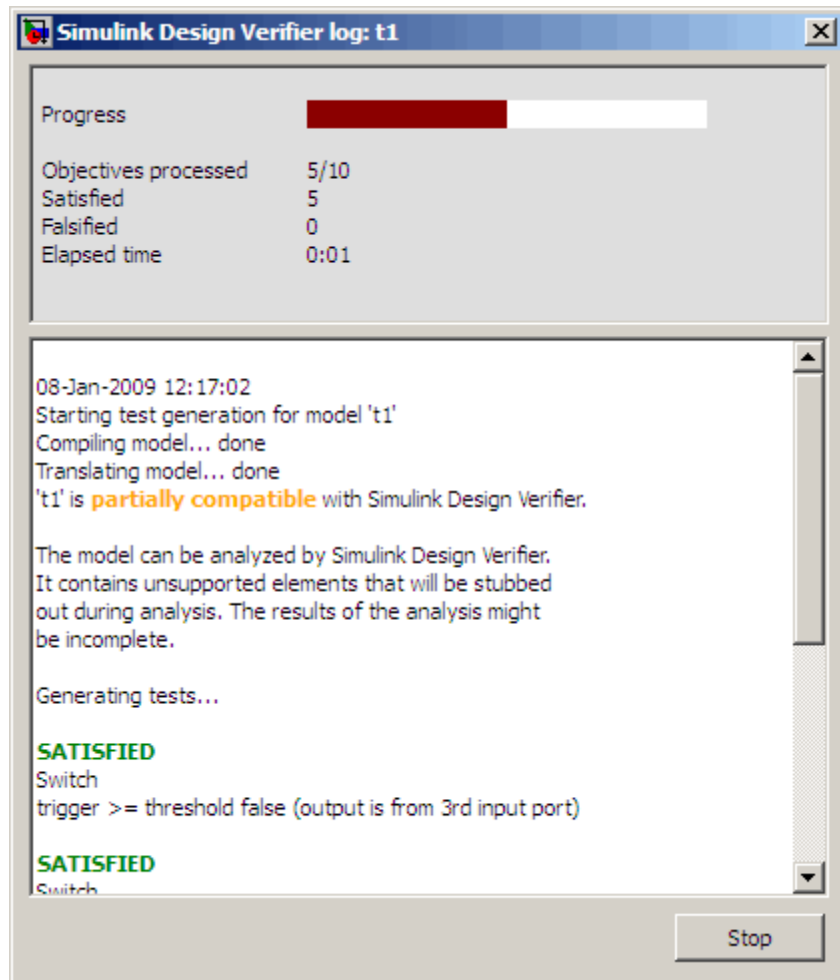


Turning On Automatic Stubbing

There are two ways to turn on automatic stubbing:

- If you have not turned on automatic stubbing and the analysis finds at least one incompatibility, the analysis stops and asks if you want to turn on automatic stubbing. Click **Continue** to proceed with the analysis.

- Before starting the analysis, in the Configuration Parameters dialog box, on the main Design Verifier pane, select **Automatic stubbing of unsupported block and functions**. When you run the analysis, you are notified that stubbing is turned on and the analysis continues.



Reviewing the Results

If you ran the analysis with automatic stubbing enabled, make sure to review the results. In this report, you see a table of unsupported blocks that the software encountered.

Unsupported Blocks

The following blocks are not supported by Simulink Design Verifier. They were abstracted during the analysis. This can lead Simulink Design Verifier to produce only partial results for parts of the model that depends on the output values of these blocks.

Block	Type
Trigonometric Function	Trigonometry

The Summary report for the t1 example model shows that one objective was satisfied without generating a test case. The software cannot generate the test case because it does not understand the operation of the Trigonometric Function block.

Chapter 1. Summary

Analysis Information

Model:	t1
Mode:	TestGeneration
Status:	Completed normally

Objectives Status

Number of Objectives:	10
Objectives Satisfied:	9
Objectives Satisfied - No Test Case:	1

Achieving Complete Results

If your analysis does not achieve complete results because of the stubbing, you can define custom block replacements to give a more precise definition of the unsupported blocks. For more information:

- “Defining Custom Block Replacements” on page 4-7.
- Enter

```
echodemo sldvdemo_blockreplacement_unsupportedblocks
```

to step through the “Block Replacements for Unsupported Models” demo.

Approximations

In this section...
“Approximations During Model Analysis” on page 2-14
“Types of Approximations” on page 2-14
“Converting Floating-Point Arithmetic to Rational-Number Arithmetic ” on page 2-14
“Linearizing 2-D Lookup Tables” on page 2-15
“Unrolling While Loops” on page 2-15
“Ensuring the Validity of the Analysis” on page 2-15

Approximations During Model Analysis

The Simulink Design Verifier software attempts to generate inputs and parameters to achieve test and proof objectives. However, there could be an infinite number of values for the software to search. To create reasonable limits on the analysis, the software performs approximations to simplify the analysis. The software records any approximations it performed in the Analysis Information chapter of the Simulink Design Verifier HTML report.

Types of Approximations

Simulink Design Verifier software performs three types of approximations when it analyzes a model:

- “Converting Floating-Point Arithmetic to Rational-Number Arithmetic ” on page 2-14
- “Linearizing 2-D Lookup Tables” on page 2-15
- “Unrolling While Loops” on page 2-15

Converting Floating-Point Arithmetic to Rational-Number Arithmetic

The Simulink Design Verifier software simplifies the linear arithmetic of floating-point numbers by approximating them with infinite-precision rational numbers. The software discovers how the logical relationships between

these values affects the proof and test objectives. This analysis enables the software to support supervisory logic that is commonly found in embedded controls designs.

If your model contains floating-point values in the signals, input values, or block parameters, the Simulink Design Verifier software converts those values to rational numbers before performing its analysis.

Note As a result of these approximations, Simulink Design Verifier software does not consider the effect of round-off error, or the upper and lower bounds of floating-point numbers.

Linearizing 2-D Lookup Tables

The Simulink Design Verifier software does not support nonlinear arithmetic. If your model contains any Lookup Table (2-D) blocks, the software approximates nonlinear 2-D interpolation with linear interpolation by fitting planes to each interpolation interval, if necessary.

Unrolling While Loops

If your model or any Stateflow chart in your model contains a while loop, the Simulink Design Verifier software tries to find a bound that allows the while loop to exit. To find a bound, it unrolls the while loop and executes it three times. If the software does not find a bound for a test case generation analysis, it sets the number of loop iterations to three for the purpose of the analysis. If you are performing a property-proving analysis, the analysis terminates.

Ensuring the Validity of the Analysis

The Simulink Design Verifier software records all approximations it performed in the Analysis Information chapter of the HTML report. (For a description of the contents of this chapter, see “Analysis Information Chapter” on page 9-20.)

Review the analysis results carefully when the software uses approximations. Evaluate your model to identify which blocks or subsystems caused the software to perform the approximations.

In rare cases, an approximation can result in test cases that fail to achieve test objectives, or counterexamples that fail to falsify proof objectives. For example, suppose the software generates a test case signal that should achieve an objective by exceeding a threshold; a floating-point round-off error might prevent that signal from attaining the threshold value.

Ensuring Compatibility with the Simulink Design Verifier Software

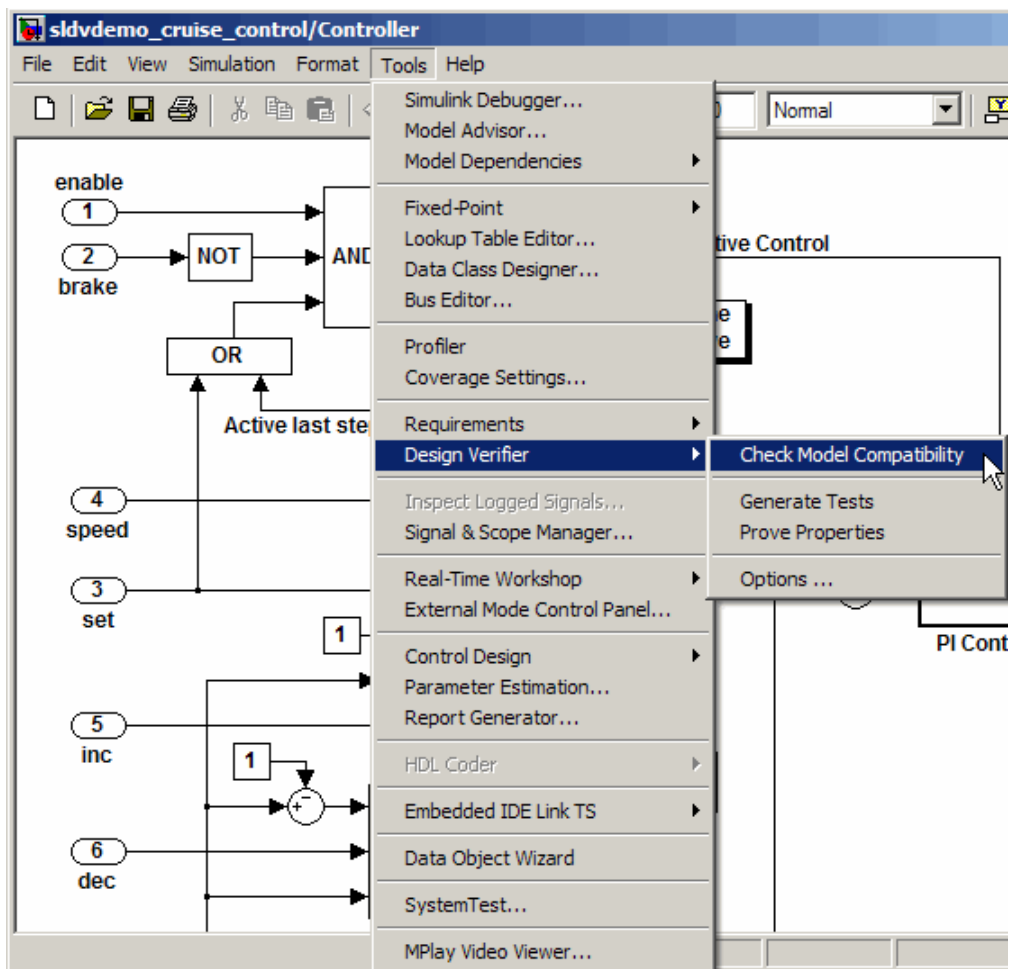
The Simulink Design Verifier software supports a broad range of Simulink and Stateflow software features. However, there are features that the product does not support. Therefore, you must avoid using particular features in models that you plan to analyze with the Simulink Design Verifier software. The following sections identify the unsupported features and describe how to check whether your model is compatible for use with the Simulink Design Verifier software.

- “Checking Model Compatibility” on page 3-2
- “Unsupported Simulink Software Features” on page 3-8
- “Unsupported Stateflow Software Features” on page 3-12
- “Support Limitations for the Embedded MATLAB Subset” on page 3-14
- “Fixed-Point Support Limitations” on page 3-17

Checking Model Compatibility

The Simulink Design Verifier software automatically checks the compatibility of your model before it begins the analysis.

In addition, the software runs the same check before analyzing the model. To run this check, in the model window, select **Tools > Design Verifier > Check Model Compatibility**.



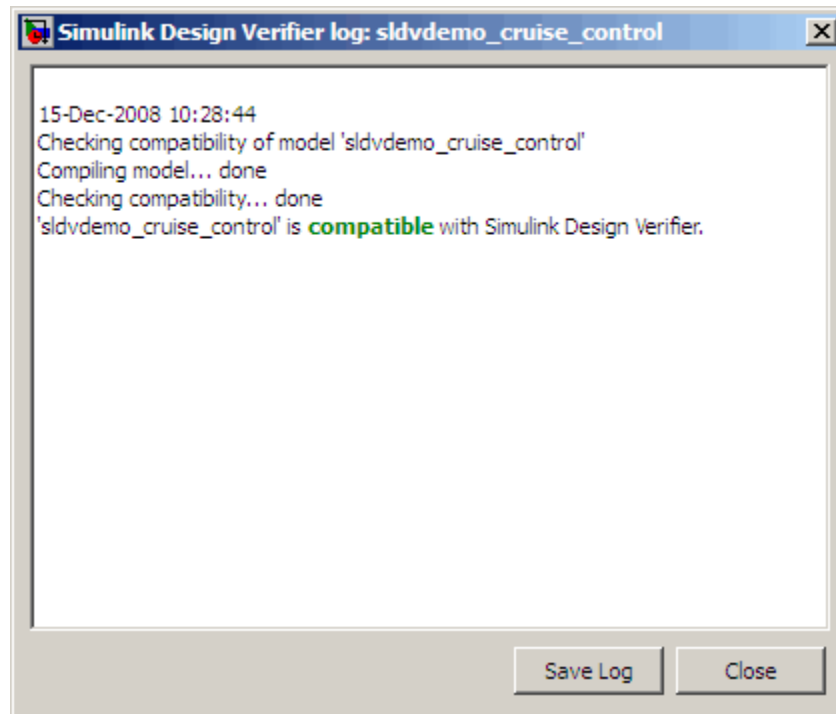
Alternatively, you can use the `sldvcompat` function to run the compatibility checker programmatically at the command line or in an M-file program. For more information, see the `sldvcompat` reference page.

There are three outcomes of a compatibility check:

- “Model Is Compatible” on page 3-3
- “Model Is Incompatible” on page 3-4
- “Some Model Elements Are Incompatible” on page 3-5

Model Is Compatible

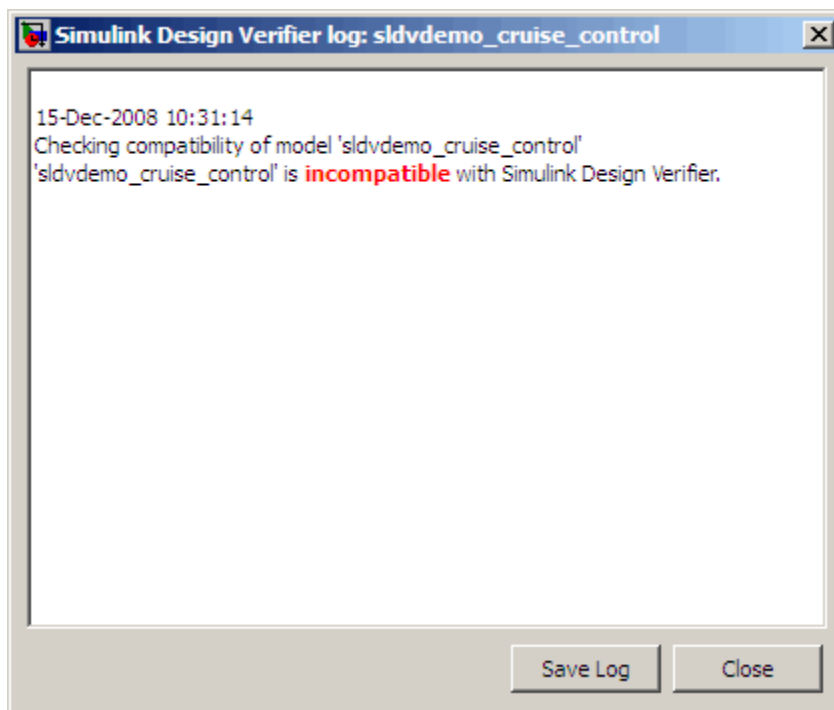
In the log window, you see if your model is compatible with the Simulink Design Verifier software.



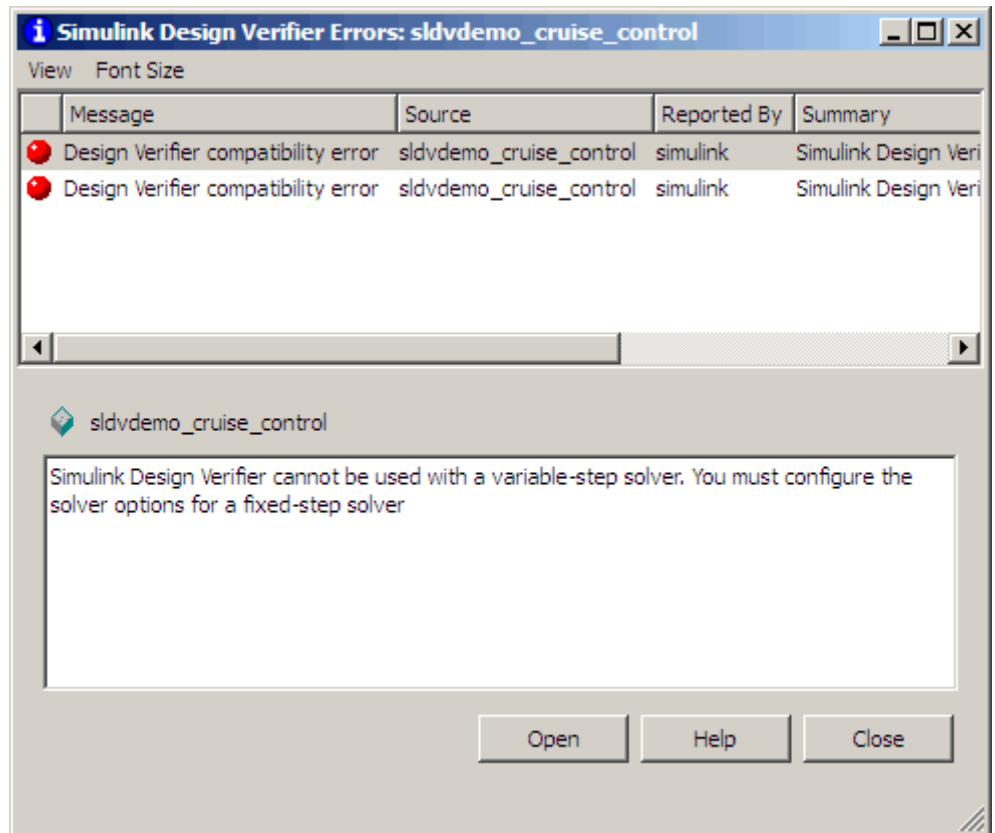
Model Is Incompatible

If the model itself is incompatible with the software, for example, if it uses a variable-step solver, you see two dialog boxes:

- Simulink Design Verifier log



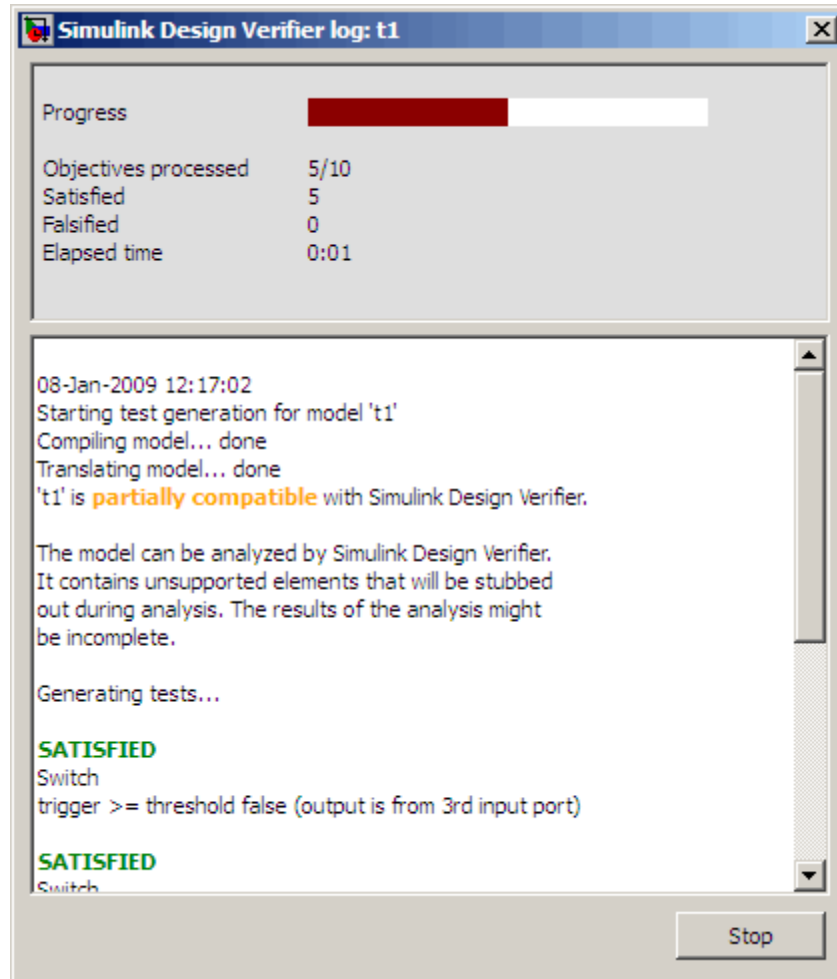
- Simulation Diagnostics Viewer. Use the information in this dialog box to identify and correct the incompatibility.



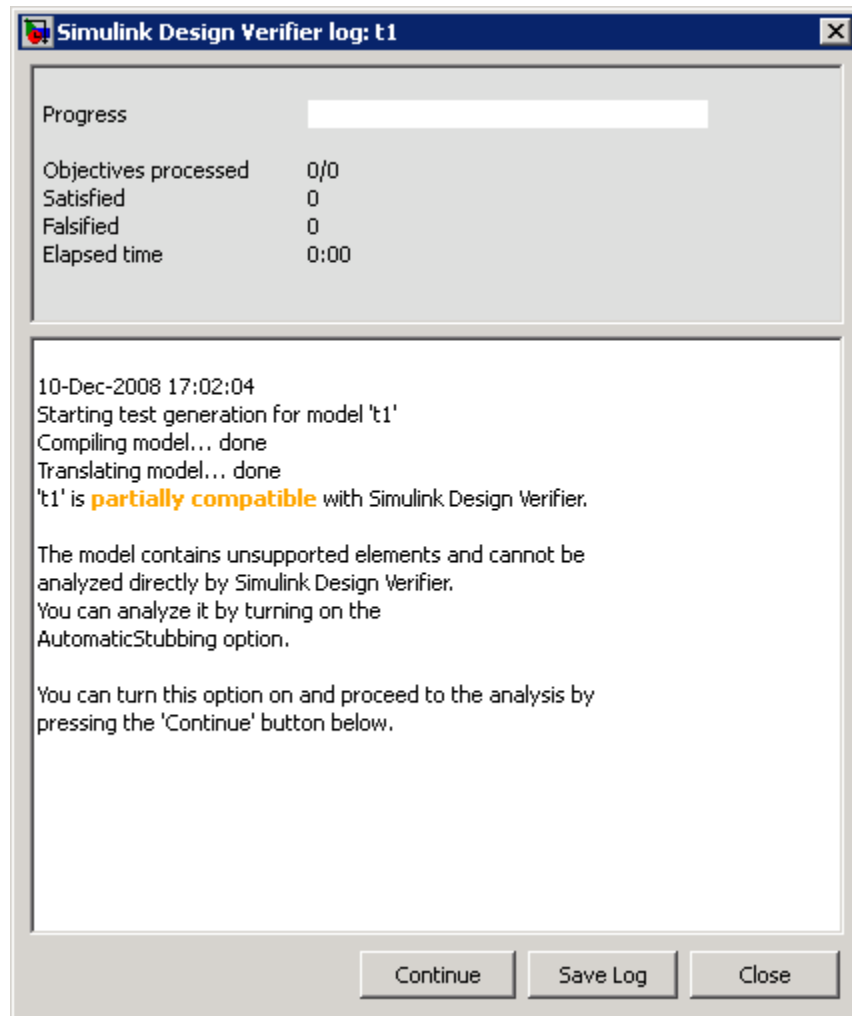
Note For more information about this dialog box, see “Simulation Diagnostics Viewer” in the *Simulink User’s Guide*.

Some Model Elements Are Incompatible

If at least one element in the model is incompatible, you see a notification in the Simulink Design Verifier log window. If you have turned on automatic stubbing, the analysis proceeds.



If you have not turned on automatic stubbing, the analysis stops. You see a query asking if you want to turn it on so that the analysis can proceed.



Note For instructions on how to use automatic stubbing, see “Handling Incompatibilities with Automatic Stubbing” on page 2-6.

Unsupported Simulink Software Features

In this section...
“Simulink Software Features Not Supported” on page 3-8
“Simulink Block Support Limitations” on page 3-9

Simulink Software Features Not Supported

The Simulink Design Verifier software does not support the following Simulink software features. Avoid using these unsupported features in models that you analyze with the Simulink Design Verifier software.

Not Supported	Description
Variable-step solvers	The Simulink Design Verifier software supports only fixed-step solvers. (See “Choosing a Fixed-Step Solver” in the <i>Simulink User’s Guide</i> .)
Complex signals	The Simulink Design Verifier software supports only real signals. (For contrast, see “Complex Signals” in the <i>Simulink User’s Guide</i> .)
Enumerated data types	The Simulink Design Verifier software does not support enumerated data types.
Multiword fixed-point data types	The Simulink Design Verifier software does not support multiword fixed-point data types.

Not Supported	Description
Signals with nonzero sample time offset	The Simulink Design Verifier software does not support models with signals that have nonzero sample time offsets.
Nonzero start times	<p>Although Simulink allows you to specify a nonzero simulation start time, the Simulink Design Verifier software generates signal data that begins only at zero. If your model specifies a nonzero start time:</p> <ul style="list-style-type: none"> • If you do not select the Reference input model in generated harness parameter (the default), the harness model is a subsystem. The software sets the start time of the harness model to 1 and continues the analysis. • If you select the Reference input model in generated harness parameter, a Model block references the harness model. The Simulink Design Verifier software cannot change the start time of the harness model, so the analysis stops and you see a recommendation to set the Start time parameter to 0.

Simulink Block Support Limitations

The Simulink Design Verifier software provides various levels of support for Simulink blocks. The software either fully or partially supports particular blocks. It does not support other blocks.

If your model contains unsupported blocks, you can turn on automatic stubbing, which considers the interface of the unsupported blocks, but not their behavior. However, if any of the unsupported blocks affect the simulation outcome, the analysis may achieve only partial results. For details about automatic stubbing, see “Handling Incompatibilities with Automatic Stubbing” on page 2-6.

To guarantee 100% coverage, avoid using unsupported blocks in models that you analyze with the Simulink Design Verifier software.

Similarly, specify only the block parameters that the Simulink Design Verifier software recognizes for blocks that it partially supports. See Chapter 14, “Simulink Block Support”.

Limitations of Support for Model Reference

The Simulink Design Verifier software supports the Model block, but with the following limitations. The software cannot analyze a model that contains one or more Model blocks if:

- The parent model or any of the referenced models gives an error when one of the following model parameters is set to Error:
 - **Diagnostics > Connectivity > Element name mismatch**
 - **Diagnostics > Connectivity > Mux blocks used to create bus signals**

You can use the **Element name mismatch** diagnostic along with bus objects to ensure that your model meets bus element naming requirements imposed by some blocks.

If your model contains Mux blocks that create bus signals, refer to “Tips” in “Mux blocks used to create bus signals” to resolve this problem.

- A referenced model references a variable in its workspace that is either defined in its own workspace or in the base MATLAB workspace, and it is also defined with the same name in the parent model’s workspace. Rename the variable used by the referenced model to a unique name so that you can analyze the model.

Exception: If the parent model and a referenced model both define an instance of a `Simulink.Signal` object used as local data storage with the same name, the software can analyze the model.

- Any of the models in the model reference hierarchy have algebraic loops that cannot be eliminated with algebraic loop minimization. If you encounter this limitation, set the **Minimize algebraic loop** parameter on the **Diagnostics** pane of the Configuration Parameters dialog box to Error. Then, update the model to identify the location of algebraic loop in the model.

To eliminate this problem so that the software can analyze the model, break any algebraic loops with Unit Delay blocks to ensure that the execution order is predictable.

For more information, see “Algebraic Loops” in the *Simulink User’s Guide*.

Unsupported Stateflow Software Features

The Simulink Design Verifier software does not support the following Stateflow software features. Avoid using these unsupported features in models that you analyze with the Simulink Design Verifier software.

Not Supported	Description
<p>m1 namespace operator, m1 function, m1 expressions</p>	<p>The Simulink Design Verifier software does not support calls to MATLAB functions or access to MATLAB workspace variables, which the Stateflow software allows (see “Using MATLAB Functions and Data in Actions” in the <i>Stateflow and Stateflow® Coder™ User’s Guide</i>).</p>
<p>C math functions</p>	<p>The Simulink Design Verifier software supports calls to the following C math functions: <code>abs</code>, <code>ceil</code>, <code>fabs</code>, <code>floor</code>, <code>fmod</code>, <code>labs</code>, <code>ldexp</code>, and <code>pow</code> (only for an integer exponent).</p> <p>The software does not support calls to other C math functions that the Stateflow software allows. Turning on automatic stubbing allows these functions to be eliminated during the analysis. For details about automatic stubbing, see “Handling Incompatibilities with Automatic Stubbing” on page 2-6.</p> <p>For information about C math functions in Stateflow, see “Calling C Functions in Actions” in the <i>Stateflow and Stateflow Coder User’s Guide</i></p>

Not Supported	Description
Recursion	The Simulink Design Verifier software does not support recursive functions, which the Stateflow software allows you to implement using graphical functions (see “Using Graphical Functions to Extend Actions” in the <i>Stateflow and Stateflow Coder User’s Guide</i>). Also, the Simulink Design Verifier software does not support recursion that the Stateflow software allows you to implement using a combination of event broadcasts and function calls.
Custom C or C++ code	The Simulink Design Verifier software does not support custom C or C++ code, which the Stateflow software allows (see “Building Targets” in the <i>Stateflow and Stateflow Coder User’s Guide</i>).
Machine-parented data and events	The Simulink Design Verifier software does not support machine-parented data and events (i.e., defined at the level of the Stateflow machine in the Stateflow hierarchy), which the Stateflow software allows (see “Defining Data” and “Defining Events” in the <i>Stateflow and Stateflow Coder User’s Guide</i>).
Absolute-time temporal logic	The Simulink Design Verifier software does not support absolute-time temporal logic, which the Stateflow software allows (see “Operators for Absolute-Time Temporal Logic” in the <i>Stateflow and Stateflow Coder User’s Guide</i>).

Support Limitations for the Embedded MATLAB Subset

In this section...
“Unsupported Embedded MATLAB Subset Features” on page 3-14
“Limitations of Embedded MATLAB Library Function Support” on page 3-15

Unsupported Embedded MATLAB Subset Features

The Simulink Design Verifier software does not support the following features of the Embedded MATLAB™ Function block in the Simulink software and Embedded MATLAB functions in the Stateflow software. Avoid using these unsupported features in models that you analyze with the Simulink Design Verifier software.

Not Supported	Description
Complex numbers	The Simulink Design Verifier software supports only real numbers. The Embedded MATLAB subset also supports complex numbers. For more information, see “Working with Complex Numbers” in the <i>Embedded MATLAB™ User’s Guide</i> .
Characters	The Simulink Design Verifier software does not support characters, which the Embedded MATLAB subset allows. For more information, see “Working with Characters” in the <i>Embedded MATLAB™ User’s Guide</i> .

Not Supported	Description
C functions	<p>The Simulink Design Verifier software does not support calls to external C functions, which the Embedded MATLAB subset allows.</p> <p>For more information about the Embedded MATLAB subset, see “Calling C Functions from the Embedded MATLAB Subset” in the <i>Embedded MATLAB™ User’s Guide</i>.</p>
Extrinsic functions	<p>The Simulink Design Verifier software supports extrinsic functions only when they do not affect the output of an Embedded MATLAB function.</p> <p>For more information about calling extrinsic functions, see “Calling MATLAB Functions” in the <i>Embedded MATLAB™ User’s Guide</i>.</p>

Limitations of Embedded MATLAB Library Function Support

The Simulink Design Verifier software provides various levels of support for Embedded MATLAB library functions. The software either fully or partially supports particular functions. It does not support other functions.

If your model contains unsupported functions, you can turn on automatic stubbing, which considers the interface of the unsupported functions, but not their behavior. However, if any of the unsupported functions affect the simulation outcome, the analysis may achieve only partial results. For details about automatic stubbing, see “Handling Incompatibilities with Automatic Stubbing” on page 2-6.

To guarantee 100% coverage, avoid using unsupported Embedded MATLAB library functions in models that you analyze with the Simulink Design Verifier software.

Avoid using unsupported Embedded MATLAB library functions in models that you analyze with the Simulink Design Verifier software. See Chapter 15, “Embedded MATLAB Subset Support” for a list of the Embedded MATLAB

library functions for which the Simulink Design Verifier software provides limited or no support.

Fixed-Point Support Limitations

The Simulink Design Verifier software supports fixed-point data types in models that it analyzes, with one exception. Parameter configurations do not support fixed-point data types. For more information about configuring Simulink Design Verifier parameters, see Chapter 5, “Specifying Parameter Configurations”.

For detailed information about these limitations, see “Tunable Expression Limitations” in the *Real-Time Workshop® User’s Guide*.

Working with Block Replacements

With the Simulink Design Verifier software, you can define rules to replace blocks automatically in your model. For example, you can work around a block that is incompatible with the software by creating a rule that replaces an unsupported Simulink block in your model with a supported block that is functionally equivalent. Or, you can customize blocks for analysis by creating a rule that adds constraints or objectives to particular blocks in your model. The following sections introduce block replacements and illustrate a process for writing block replacement rules.

- “About Block Replacements” on page 4-2
- “Built-In Block Replacements” on page 4-3
- “Template for Block Replacement Rules” on page 4-6
- “Defining Custom Block Replacements” on page 4-7
- “Executing Block Replacements” on page 4-15

About Block Replacements

The Simulink Design Verifier software can perform automatic block replacements in a model. It can replace instances of a particular block in your model with an entirely different block from an existing library or from a block library that you create. When performing block replacements, the software copies your model and replaces blocks in the copy, without altering your original model. In this way, you can easily customize a model for analysis.

The Simulink Design Verifier software replaces blocks automatically in a model using:

- Libraries of replacement blocks
- Rules that define which blocks to replace and under what conditions

You replace any block with any built-in block, library block, or subsystem.

Block replacements are extensible, allowing you to define your own libraries of replacement blocks and custom block replacement rules. Use this capability if you need to:

- Work around an incompatibility, such as the presence of unsupported blocks in your model.
- Customize a block for analysis, such as adding constraints to its input signals, objectives to its output signals, or eliminating the contents of a subsystem or Model block to simplify your analysis.

Note You can use automatic stubbing as an alternative to block replacements. Automatic stubbing replaces unsupported blocks with elements that have the same interface. For more information, see “Handling Incompatibilities with Automatic Stubbing” on page 2-6.

Built-In Block Replacements

The Simulink Design Verifier software provides a set of block replacement rules and a corresponding library of replacement blocks. Use these built-in block replacements when analyzing models. They serve as examples that you can examine to learn how to create your own block replacements.

The following table lists the factory default block replacement rules, available in the `matlabroot\toolbox\sldv\sldv\private` directory. There are two implementations of each factory default block replacement rule. Rules whose file names end with `_normal.m` replace blocks with Subsystem blocks. Rules whose file names end with `_configss.m` replace blocks with Configurable Subsystem blocks.

File Name	Description
blkrep_rule_lookup_normal.m blkrep_rule_lookup_configss.m	A rule that replaces Lookup Table blocks with an implementation that includes test objectives for each breakpoint and interval specified by the Vector of input values parameter.
blkrep_rule_lookup2D_normal.m blkrep_rule_lookup2D_configss.m	A rule that adds Test Condition/Proof Assumption blocks to the input ports of Lookup Table (2-D) blocks. Each Test Condition/Proof Assumption block constrains signal values to the interval specified by the corresponding breakpoint vector.
blkrep_rule_mpswitch2_normal.m blkrep_rule_mpswitch2_configss.m	A rule that adds a Test Condition/Proof Assumption block to the control input port of Multiport Switch blocks whose Number of inputs parameter is 2. The Test Condition/Proof Assumption block constrains signal values to the interval [1, 2] (or [0, 1] if the block uses zero-based indexing).

File Name	Description
blkrep_rule_mpswitch3_normal.m blkrep_rule_mpswitch3_configss.m	A rule that adds a Test Condition/Proof Assumption block to the control input port of Multiport Switch blocks whose Number of inputs parameter is 3. The Test Condition/Proof Assumption block constrains signal values to the interval [1, 3] (or [0, 2] if the block uses zero-based indexing).
blkrep_rule_mpswitch4_normal.m blkrep_rule_mpswitch4_configss.m	A rule that adds a Test Condition/Proof Assumption block to the control input port of Multiport Switch blocks whose Number of inputs parameter is 4. The Test Condition/Proof Assumption block constrains signal values to the interval [1, 4] (or [0, 3] if the block uses zero-based indexing).
blkrep_rule_mpswitch5_normal.m blkrep_rule_mpswitch5_configss.m	A rule that adds a Test Condition/Proof Assumption block to the control input port of Multiport Switch blocks whose Number of inputs parameter is 5. The Test Condition/Proof Assumption block constrains signal values to the interval [1, 5] (or [0, 4] if the block uses zero-based indexing).
blkrep_rule_switch_normal.m blkrep_rule_switch_configss.m	A rule that replaces Switch blocks with an implementation that includes test objectives, requiring that each switch position be exercised when the values of the first and third input ports are different.

File Name	Description
blkrep_rule_selector IndexVecPort_normal.m blkrep_rule_selector IndexVecPort_configss.m	A rule that adds a Test Condition/Proof Assumption block to the index port of Selector blocks whose Index Option parameter is Index vector (port) . The Test Condition/Proof Assumption block constrains signal values to an interval whose endpoints are derived from the values of the Selector block's Input port size and Index mode parameters.
blkrep_rule_selector StartingIdxPort_normal.m blkrep_rule_selector StartingIdxPort_configss.m	A rule that adds a Test Condition/Proof Assumption block to the index port of Selector blocks whose Index Option parameter is Starting index (port) . The Test Condition/Proof Assumption block constrains signal values to an interval whose endpoints are derived from the values of the Selector block's Input port size , Output size , and Index mode parameters.

You can find the library of replacement blocks that corresponds to the factory default rules at:

`matlabroot/toolbox/sldv/sldv/sldvblockreplacementlib.mdl`

Template for Block Replacement Rules

To help you create block replacement rules, the Simulink Design Verifier software provides an annotated M-file template that contains a skeleton implementation of the requisite callbacks. You can find the template at:

```
matlabroot/toolbox/sldv/sldv/sldvblockreplacetemplate.m
```

To create a block replacement rule, make a copy of the template and edit the copy for the behavior that you want for the rule you are creating. For information on how to implement your rule, see the comments in the template. For information on using the template to write custom block replacements rules, see “Writing Block Replacement Rules” on page 4-10.

Defining Custom Block Replacements

In this section...

“About Custom Block Replacements” on page 4-7

“Specifying Replacement Blocks” on page 4-7

“Writing Block Replacement Rules” on page 4-10

About Custom Block Replacements

Defining custom block replacements in the Simulink Design Verifier software consists of the following tasks:

- “Specifying Replacement Blocks” on page 4-7
- “Writing Block Replacement Rules” on page 4-10

Specifying Replacement Blocks

A replacement block can be one of the built-in blocks in the Simulink model library or a block in a user-created library.

In the Simulink Design Verifier software, replacement blocks have the following restrictions:

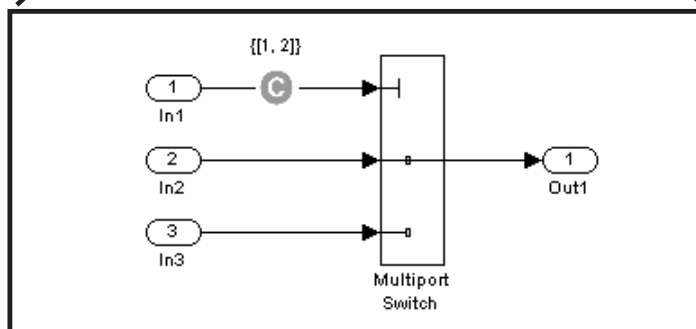
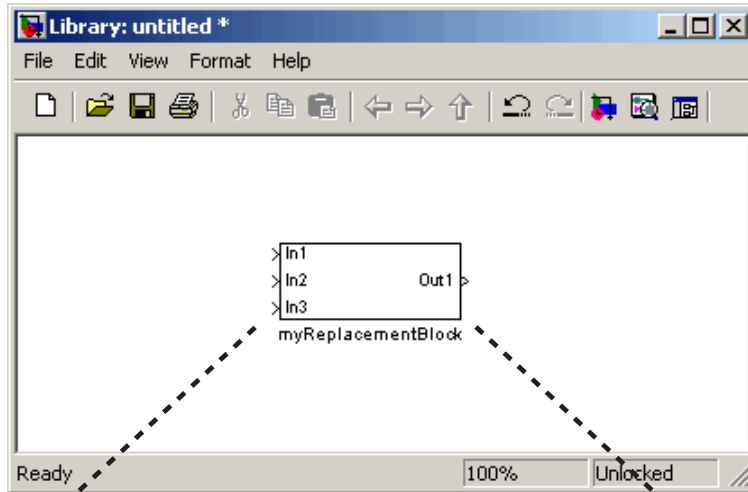
- They must be built-in blocks or subsystems.
- They cannot be Model blocks, nor can they include any Model blocks.

Note A Model block cannot be a replacement block, but you can replace Model blocks with built-in blocks or subsystems.

- They must reside in a block library that is available on your MATLAB search path.
- If the replacement block is a subsystem, it must contain Inport and Outport blocks that have the default names (In1 and Out1).

To create a user library and specify a replacement block as a masked subsystem:

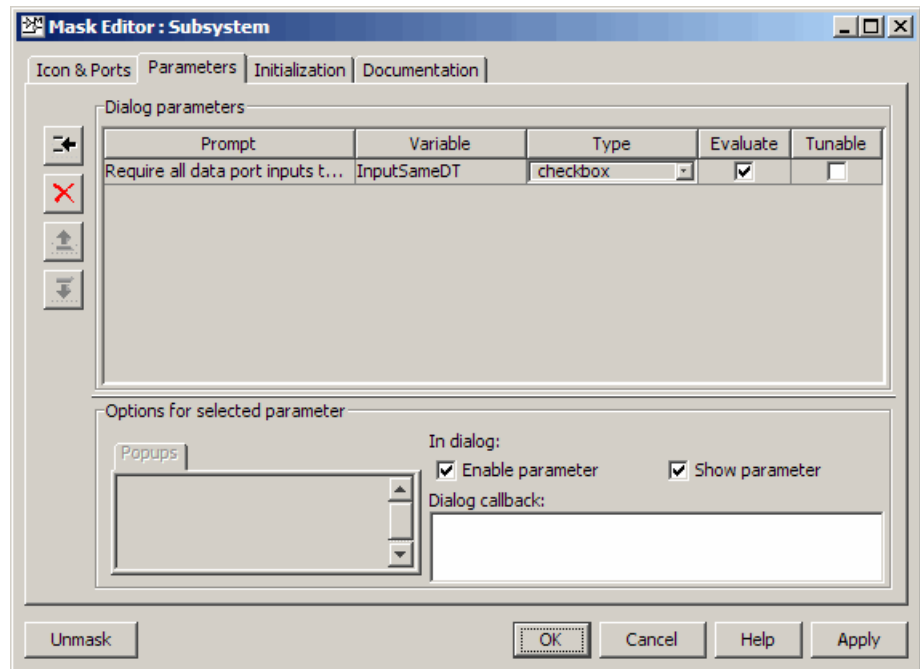
- 1 In the Simulink Library Browser, select **File > New > Library**.
- 2 In your library, create a subsystem named `myReplacementBlock` to represent your replacement block. It should look like the following graphic, with several parameters set:
 - In the Multiport Switch block, set the **Number of inputs** parameter to 2.
 - In the Test Condition block, set the **Values** parameter to `{[1, 2]}`.



- 3** To create a mask for your subsystem, select the subsystem, right-click, and select **Mask subsystem** from the context menu. For information and a tutorial for creating block masks, see “Working with Block Masks” in the *Simulink User’s Guide*.

For this example, the masked subsystem includes the following specifications in its Mask Editor:

- The **Parameters** pane defines a mask parameter named InputSameDT, which replicates the behavior of the **Require all data port inputs to have the same data type** parameter of the underlying Multiport Switch block.



Note When you create mask parameters that control the behavior of parameters associated with their underlying blocks, specify actual parameter names as dialog box variables in the Mask Editor. For instance, `InputSameDT` is the actual parameter name that controls the **Require all data port inputs to have the same data type** parameter of the Multiport Switch block; therefore, it specifies the name of the dialog box variable in this example.

- In the **Initialization** pane, in the **Initialization commands** field, you see the following commands:

```
maskInputSameDT = get_param(gcf, 'InputSameDT');
blkName = sprintf('/Multiport\nSwitch');
targetBlock = [gcb, blkName];
set_param(targetBlock, 'InputSameDT', maskInputSameDT);
```

- 4 Save your block library as `custom_rule.mdl` in a directory on your MATLAB search path.

After constructing your replacement block, you can write a custom block replacement rule.

Writing Block Replacement Rules

In the Simulink Design Verifier software, block replacement rules have the following restrictions:

- The M-file that represents a block replacement rule must include particular callbacks. The MathWorks recommends that you use the block replacement rule template as a starting point for writing a custom rule. (See “Template for Block Replacement Rules” on page 4-6.)
- The M-file that represents a block replacement rule must be on the MATLAB search path.
- You cannot create a rule that replaces Inport, Outport, or Subsystem blocks in your model.

To write a rule for the replacement block:

- 1 Copy the block replacement rule template

```
matlabroot/toolbox/sldv/sldv/sldvblockreplacetemplate.m
```

- 2 Save it as `custom_rule_switch.m`.

Note For steps 2 through 10, edit the copy of the template that you saved.

- 3 Rename the function, as defined on the first line of the M-file. The function name must match its file name, without the `.m` extension. Optionally, you can edit the comments that follow the function declaration to create your own M-file help for this rule.

In this example, the first few lines of `custom_rule_switch.m` declare the function and its M-file help:

```
function rule = custom_rule_switch
%CUSTOM_RULE_SWITCH Custom block replacement rule for
%the Simulink Design Verifier software
%
% This block replacement rule identifies Multiport
% Switch blocks whose "Number of inputs" parameter
% specifies '2' and "Use zero-based indexing" parameter
% specifies 'off'. It replaces such blocks with an
% implementation that includes a Test Condition block
% on the control input signal.
```

- 4 Identify the type of block that you want to replace in your model by specifying its `BlockType` parameter as the `rule.blockType` object. Consider using the `get_param` function to obtain the value of the `BlockType` parameter for the block that you want to replace. Alternatively, you can determine this value by referring to “Block-Specific Parameters” in the *Simulink Reference*.

This example replaces Multiport Switch blocks. The `rule.blockType` object specifies the appropriate `BlockType` parameter:

```
%% Target Block Type
%
```

```
rule.BlockType = 'MultiPortSwitch';
```

- 5 Identify the replacement block by specifying its full block path name as the `rule.ReplacementPath` object. Consider using the `gcb` function as a way to get the full block path name.

This example replaces Multiport Switch blocks with the replacement block developed in “Specifying Replacement Blocks” on page 4-7. The `rule.ReplacementPath` object specifies the full block path name:

```
%% Replacement Library
%
rule.ReplacementPath = sprintf('custom_rule/myReplacementBlock');
```

- 6 Identify the type of subsystem that the Simulink Design Verifier software uses when replacing blocks by specifying a value for the `rule.ReplacementMode` object. Valid values are:
 - **Normal** — When using this rule, the software replaces blocks with a copy of the subsystem specified by the `rule.ReplacementPath` object.
 - **ConfigurableSubSystem** — When using this rule, the software replaces blocks with a Configurable Subsystem block. With the Configurable Subsystem block, you can choose whether it represents the subsystem specified by the `rule.ReplacementPath` object, or the original block before its replacement.

This example replaces Multiport Switch blocks with an ordinary Subsystem block:

```
%% Replacement Mode
%
rule.ReplacementMode = 'Normal';
```

- 7 Identify parameter values that the replacement blocks inherit from the blocks being replaced. You achieve inheritance by mapping the parameter names in a structure. Each field of the structure represents a parameter that the replacement block inherits. Specify the value of each field using the token `$original.parameter$`. `parameter` is the name of the parameter that belongs to the original block. You can determine block parameter names by referring to “Model and Block Parameters” in the *Simulink Reference*.

The following example defines a structure named `parameter` that maps the `InputSameDT` parameter from the original Multiport Switch blocks to their replacement blocks:

```
%% Parameter Handling
%
parameter.InputSameDT = '$original.InputSameDT$';

% Register the parameter mapping for the rule
rule.ParameterMap = parameter;
```

- 8** To define the callback functions, keep the following lines in the file:

```
rule.IsReplaceableCallback = @replacementTestFunction;
.
.
.
rule.PostReplacementCallback = @postReplacementFunction;
```

- 9** Customize the `replacementTestFunction` subfunction by specifying conditions under which the Simulink Design Verifier software replaces blocks in your model.

The following example instructs the Simulink Design Verifier software to replace only the Multiport Switch blocks whose `NumInputPorts` parameter is 2 and whose `zeroidx` parameter is off:

```
function out = replacementTestFunction(blockH)
% Specify the logic that determines when the Simulink Design
% Verifier software replaces a block in your model. For example,
% restrict replacements to only the blocks whose parameters
% specify particular values.
out = false;
numInputPorts = eval(get_param(blockH,'NumInputPorts'));
zeroIdx = eval(get_param(blockH,'zeroidx'));
if numInputPorts==2 && zeroIdx=='off',
    out = true;
end
```

- 10** Optionally, you can customize the `postReplacementFunction` subfunction to specify the actions the software performs after a block has been replaced.

For an example of a `postReplacementFunction` subfunction, open the following file:

```
matlabroot/toolbox/sldv/sldv/blkrep_rule_selectorIndexVecPort_normal.m
```

11 Save the edited M-file.

After constructing a replacement block and writing its corresponding block replacement rule, you can execute your custom block replacement.

Executing Block Replacements

In this section...

“Configuring Block Replacements” on page 4-15

“Replacing Blocks in a Model” on page 4-16

Configuring Block Replacements

You must configure block replacement options before executing block replacements in your model. To specify block replacement options from the model window:

- 1 Open the `sldvdemo_cruise_control` model.
- 2 Save a copy of this model and name it `my_sldvdemo_cruise_control`.
- 3 From the **Tools** menu of your Simulink model, select **Design Verifier > Options**.

The Configuration Parameters dialog box displays the main pane of the **Design Verifier** category.

- 4 In the **Select** tree of the Configuration Parameters dialog box, click the **Block Replacements** category.
- 5 On the Block Replacements pane, select **Apply block replacements** to enable block replacements.

Enabling this option provides access to the **List of block replacement rules (in order of priority)** and **File path of the output model** options.

- 6 In the **List of block replacement rules (in order of priority)** box, enter file names for the block replacement rules that you want to execute. The default value, `<FactoryDefaultRules>`, executes all the factory default rules.

You can specify multiple rules as a list delimited by spaces, commas, or carriage returns. The software executes the rules in the order that you list them. For example, to execute two of the factory default rules followed

by the custom block replacement example from “Defining Custom Block Replacements” on page 4-7, enter the following file names:

```
blkrep_rule_mpswitch4_normal  
blkrep_rule_lookup_normal  
custom_rule_switch
```

Note The Simulink Design Verifier software replaces a block in your model only once. If multiple rules apply to the same block, the software replaces the block using the rule with the highest priority.

- 7** After applying the block replacement rules, in the **File path of the output model** box, enter a file name for the model that results. Optionally, include a path that is either absolute or relative to the path in the **Output directory** on the main **Design Verifier** pane.
- 8** Click **OK** to apply the changes and close the Configuration Parameters dialog box.
- 9** Save the `my_sldvdemo_cruise_control` model.

Alternatively, at the command line, you can use the `sldvoptions` function to specify the block replacement options associated with a Simulink Design Verifier options object, described in “Replacing Blocks in a Model” on page 4-16.

Replacing Blocks in a Model

After enabling the **Apply block replacements** option, you can execute block replacements in your model by starting a Simulink Design Verifier analysis. For example, to trigger block replacements and start the analysis from the Configuration Parameters dialog box, on the **Design Verifier** pane, click **Generate Test Cases**.

Note The Simulink Design Verifier software can execute block replacements only on models that do not have any saved changes.

When you are replacing blocks, the Simulink Design Verifier software copies your model and replaces blocks in the copy, without altering your original model. Upon completing its analysis, the software generates a report that displays information about the block replacements it executed.

When you enable block replacements and start the analysis, the software invokes the `sldvblockreplacement` command to copy the model and perform the block replacements, before continuing the analysis.

Alternatively, to perform only the block replacements, at the command line or from an M-file program, you can use the `sldvblockreplacement` function. You pass a handle to the model and the `sldvoptions` structure as follows:

```
opts = sldvoptions;
opts.BlockReplacement = 'on'
opts.BlockReplacementRulesList = ...
'<FactoryDefaultRules>, custom_rule_switch';
[status, newmodelH] = sldvblockreplacement('modelH', opts);
```

`modelH` is a handle to the model whose blocks you want to replace. `newmodelH` is the handle to the new model with the block replacements.

Replacing the blocks in a model before running the analysis can help you debug the custom block replacement rules. Once the block replacement rules are working as you want, you can analyze the model that contains the block replacements.

See `sldvblockreplacement` for more information.

If you execute block replacements programmatically, in the MATLAB Command Window, the Simulink Design Verifier software displays a table that lists available block replacement rules.

Configuration of available block replacement rules:

Type:	Registration M-File name:	Block types:	Priority:	Active:
Built-in	blkrep_rule_mpswitch2_normal.m	MultiPortSwitch	5	0
Built-in	blkrep_rule_mpswitch2_configss.m	MultiPortSwitch	4	0
Built-in	blkrep_rule_mpswitch3_normal.m	MultiPortSwitch	3	0
Built-in	blkrep_rule_mpswitch3_configss.m	MultiPortSwitch	6	0
Built-in	blkrep_rule_mpswitch4_normal.m	MultiPortSwitch	1	1

Built-in	blkrep_rule_mpswitch4_configss.m	MultiPortSwitch	7	0
Built-in	blkrep_rule_mpswitch5_normal.m	MultiPortSwitch	2	0
Built-in	blkrep_rule_mpswitch5_configss.m	MultiPortSwitch	8	0
Built-in	blkrep_rule_lookup_normal.m	Lookup	1	1
Built-in	blkrep_rule_lookup_configss.m	Lookup	2	0
Built-in	blkrep_rule_switch_normal.m	Switch	1	0
Built-in	blkrep_rule_switch_configss.m	Switch	2	0
Built-in	blkrep_rule_lookup2D_normal.m	Lookup2D	1	0
Built-in	blkrep_rule_lookup2D_configss.m	Lookup2D	2	0
Built-in	blkrep_rule_selectorIndexVecPort_normal.m	Selector	1	0
Built-in	blkrep_rule_selectorIndexVecPort_configss.m	Selector	2	0
Built-in	blkrep_rule_selectorStartingIdxPort_normal.m	Selector	3	0
Built-in	blkrep_rule_selectorStartingIdxPort_configss.m	Selector	4	0
Custom	custom_rule_switch.m	MultiPortSwitch	2	1

The list of available block replacement rules includes all built-in rules and any custom rules that you specified using the **List of block replacement rules (in order of priority)** option (see “Configuring Block Replacements” on page 4-15). The columns of the preceding table identify the following information:

- Type — Type of rule, either built-in or custom
- Registration M-File name — Name of the M-file that expresses the rule
- Block types — `BlockType` parameter value of the block that the rule replaces
- Priority — Priority of execution when multiple rules target the same type of block for replacement
- Active — a flag that indicates whether the rule is active (1) or ignored (0)

The Simulink Design Verifier software also displays information about the block replacements. For example, the following message indicates that the software used the `custom_rule_switch.m` rule to replace a Multiport Switch block (of the same name) at the top level of the model:

Performed block replacements:

```
Replacement rule M-file name:  Replaced block:
custom_rule_switch.m         ./Multiport Switch
```

Specifying Parameter Configurations

The Simulink Design Verifier software allows you to treat block parameters in your model as variables in its analysis. The following sections introduce parameter configurations and show how you specify constraints on block parameters.

- “About Parameter Configurations” on page 5-2
- “Template for Parameter Configurations” on page 5-3
- “Defining Parameter Configurations” on page 5-4
- “Parameter Configuration Example” on page 5-7

About Parameter Configurations

The Simulink Design Verifier software can treat block parameters in your model as variables during its analysis. For example, suppose you specify a variable that is defined in the MATLAB workspace as the value of a block parameter in your model. You can instruct the Simulink Design Verifier software to treat that parameter as another input variable in its analysis. This allows you to

- Extend the results of a proof to consider the impact of additional parameter values.
- Generate comprehensive test cases for situations in which parameter values must vary to achieve more complete coverage results (for an example, see “Parameter Configuration Example” on page 5-7).

Template for Parameter Configurations

To help you create a parameter configuration file, the Simulink Design Verifier software provides an annotated M-file template:

```
matlabroot/toolbox/sldv/sldv/sldv_params_template.m
```

Alternatively, you can access the template from the **Parameters** pane in the Simulink Design Verifier options (see “Parameters Pane” on page 6-9).

To create a parameter configuration file, make a copy of the template and edit the copy. The comments in the template explain the syntax for defining parameter configurations. For more information about defining parameter configurations, see “Defining Parameter Configurations” on page 5-4.

Defining Parameter Configurations

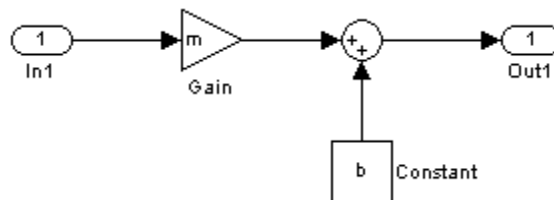
This section describes how to define parameter configurations and outlines the required syntax for their definition.

1 Define parameter configurations in an M-file function.

The Simulink Design Verifier software provides an annotated template for an M-file function that you can use as a starting point (see “Template for Parameter Configurations” on page 5-3).

2 Specify parameter configurations using a structure whose fields share the same names as the parameters that you treat as input variables.

For example, suppose you wish to constrain the **Gain** and **Constant value** parameters, *m* and *b*, which appear in the following model:



In your parameter configuration file, use the following names for the fields of the structure:

```

params.m
params.b

```

3 Constrain parameters by assigning values to the fields of the structure.

Specify points using the `Sldv.Point` constructor, which accepts a single value as its argument. Specify intervals using the `Sldv.Interval` constructor, which requires two input arguments, i.e., a lower bound and an upper bound for the interval. Optionally, you can provide one of the following strings as a third input argument that specifies inclusion or exclusion of the interval endpoints:

- '()' — Defines an open interval.

- '[' — Defines a closed interval.
- '(' — Defines a left-open interval.
- '[' — Defines a right-open interval.

Note By default, the Simulink Design Verifier software considers an interval to be closed if you omit its two-character string.

The following example constrains `m` to 3 and `b` to any value in the closed interval [0, 10]:

```
params.m = Sldv.Point(3);  
params.b = Sldv.Interval(0, 10);
```

If the parameters are scalar, you can omit the constructors and instead specify single values or two-element vectors. For instance, you can alternatively specify the previous example as:

```
params.m = 3;  
params.b = [0 10];
```

Note To indicate no constraint for an input parameter, specify `params.m = {}` or `params.m = []` in the M-file function, or omit the declaration. The Simulink Design Verifier software treats this parameter as free input and uses random parameter values.

4 Use cell arrays to specify multiple constraints for a single parameter.

You can specify multiple constraints for a single parameter by using a cell array. In this case, the Simulink Design Verifier software combines the constraints using a logical OR operation during its analysis.

The following example constrains `m` to either 3 or 5, and it constrains `b` to any value in the closed interval [0, 10]:

```
params.m = {3, 5};  
params.b = [0 10];
```

- 5 Use a 1-by- n structure to specify n sets of parameters.

You can specify several sets of parameters by expanding the size of your structure.

For instance, the following example uses a 1-by-2 structure to define two sets of parameters:

```
params(1).m = {3, 5};  
params(1).b = [0 10];  
  
params(2).m = {12, 15, Sldv.Interval(50, 60, '()')};  
params(2).b = 5;
```

The first parameter set constrains m to either 3 or 5, and it constrains b to any value in the closed interval $[0, 10]$. The second parameter set constrains m to either 12, 15, or any value in the open interval $(50, 60)$, and it constrains b to 5.

Parameter Configuration Example

In this section...
“About This Example” on page 5-7
“Constructing the Example Model” on page 5-8
“Parameterizing the Constant Block” on page 5-10
“Specifying a Parameter Configuration” on page 5-11
“Analyzing the Example Model” on page 5-13
“Simulating the Test Cases” on page 5-15

About This Example

The next five tasks describe how to create and analyze a simple Simulink model, for which you generate test cases that achieve decision coverage. However, in this example, achieving complete decision coverage is possible only when the Simulink Design Verifier software treats a particular block parameter as a variable during its analysis. Toward that end, this example explains how to specify parameter configurations for use with the Simulink Design Verifier software.

The following workflow guides you through the process of completing this example:

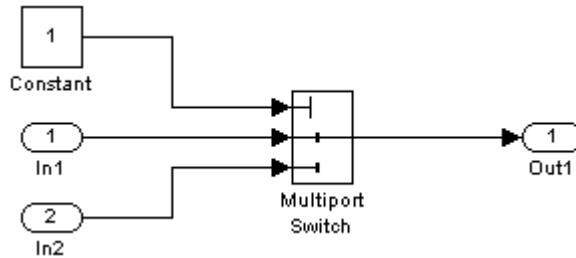
Task	Description	See...
1	Construct the example model.	“Constructing the Example Model” on page 5-8
2	Specify a variable as the value of a Constant block parameter.	“Parameterizing the Constant Block” on page 5-10
3	Constrain the value of the variable that the Constant block specifies.	“Specifying a Parameter Configuration” on page 5-11

Task	Description	See...
4	Generate test cases for your model and interpret the results.	“Analyzing the Example Model” on page 5-13
5	Simulate the test cases and measure the resulting decision coverage.	“Simulating the Test Cases” on page 5-15

Constructing the Example Model

In this task, you construct a simple Simulink model that you use throughout the remaining tasks.

- 1 Create an empty Simulink model (see “Creating an Empty Model” in *Simulink User’s Guide* for help with this step).
- 2 Copy the following blocks into your empty model window (see “Adding Blocks to Your Model” in the Simulink documentation for help with this step):
 - Two Inport blocks to initiate the input signals, from the Sources library
 - A Multiport Switch block to provide simple logic, from the Signal Routing library
 - A Constant block to control the switch, from the Sources library
 - An Outport block to receive the output signal, from the Sinks library
- 3 In your model window, double-click the Multiport Switch block to access its dialog box and specify its **Number of inputs** option as 2.
- 4 In your model window, connect the blocks so that your model looks like this (see “Connecting Blocks” in *Simulink User’s Guide* for help with this step):

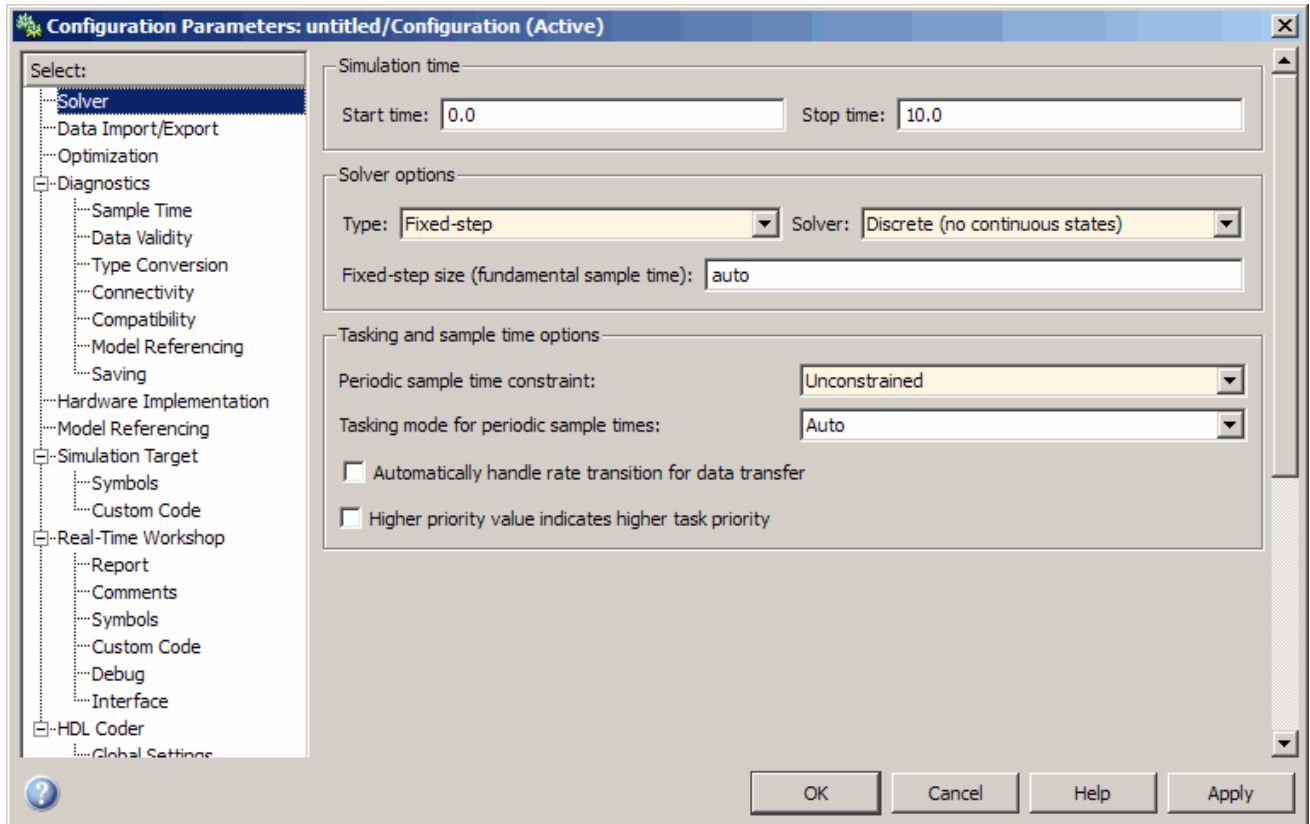


- 5 In your model window, select **Simulation > Configuration Parameters**.

The Configuration Parameters dialog box appears.

- 6 In the **Select** tree on the left side of the Configuration Parameters dialog box, click the **Solver** category. Under **Solver options** on the right side, set the **Type** option to Fixed-step, and then set the **Solver** option to Discrete (no continuous states).

The Configuration Parameters dialog box looks as follows:



7 Click **Apply** and **OK** to apply your changes and close the Configuration Parameters dialog box.

8 Save your model as `param_example.mdl` for use in the next step.

Parameterizing the Constant Block

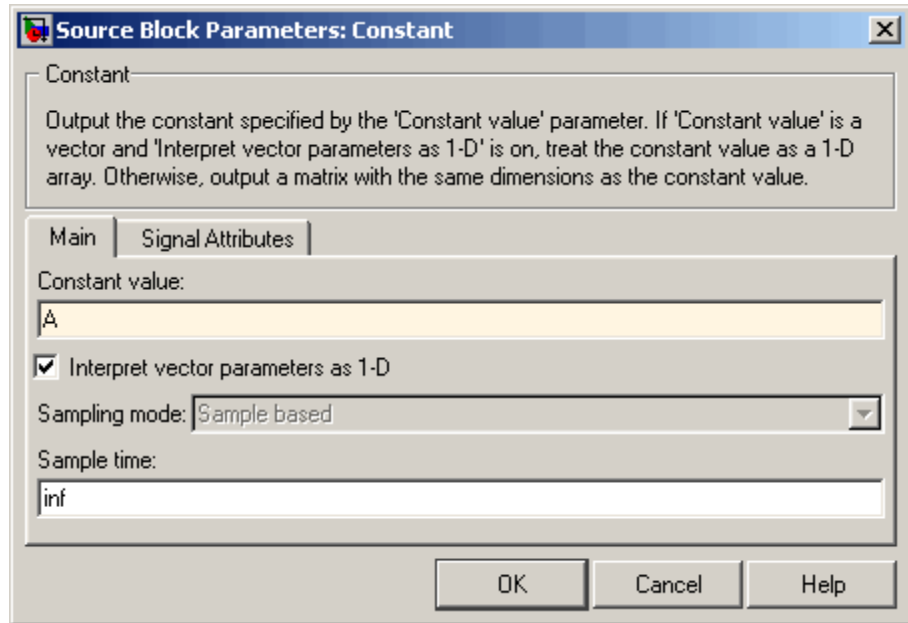
In this task, you parameterize the Constant block in your model. In particular, you specify a variable as the value of the Constant block's **Constant value** parameter.

1 In your model window, double-click the Constant block.

The Constant block parameter dialog box appears.

- 2 In the **Constant value** box, enter A.

The Constant block parameter dialog box should look as follows.



- 3 Click **OK** to apply your change and close the Constant block parameter dialog box.

- 4 In the MATLAB Command Window, enter

```
A = 1;
```

This command defines in the MATLAB workspace a variable named A whose value is 1. The Simulink software resolves the **Constant value** parameter to this variable, initializing its value for simulation.

- 5 Save your model for use in the next step.

Specifying a Parameter Configuration

In this task, you customize the parameter configuration file template so that it constrains the variable A.

- 1** In your Simulink model window, select **Tools > Design Verifier > Options**.

The Simulink Design Verifier software displays its options in the Configuration Parameters dialog box.

- 2** In the **Select** tree on the left side of the Configuration Parameters dialog box, click the **Design Verifier > Parameters** category. In the **Parameters** pane on the right side, ensure that the **Apply parameters** option is enabled.

Enabling the **Apply parameters** option provides access to the **Parameter configuration file** option.

- 3** Click **Edit** next to the **Parameter configuration file** option.

The Simulink Design Verifier software opens `sldv_params_template.m` in an editor.

- 4** Edit the template's text so that it appears as follows:

```
function params = params_example_function
    % This function defines a parameter configuration for the
    % example model that the documentation discusses.

    params.A = [1 2];
```

The preceding code renames the function as `params_example_function` and constrains parameter A to the closed interval [1 2].

- 5** Save your changes to the template as `params_example_function.m` in the same directory as the example model.
- 6** Close the MATLAB Editor.
- 7** In the Configuration Parameters dialog box, click **Browse** next to the **Parameter configuration file** option, and then select your parameter configuration file, `params_example_function.m`.
- 8** Click **Apply** and **OK** to apply your change and close the Configuration Parameters dialog box.

- 9 Save your model for use in the next step.

Analyzing the Example Model

In this task, you execute the Simulink Design Verifier analysis using the parameter configuration file you just created. The software generates test cases and produces results for you to interpret.

- 1 In your Simulink model window, select **Tools > Design Verifier > Generate Tests**.

The Simulink Design Verifier software begins analyzing your model to generate test cases. When the software completes its analysis, it generates the following items:

- Simulink Design Verifier report — The Simulink Design Verifier software displays an HTML report named `param_example_report.html`.
- Test harness — The Simulink Design Verifier software displays a harness model named `param_example_harness.mdl`.

- 2 In the Simulink Design Verifier report **Table of Contents**, click **Test Cases**.
- 3 Click **Test Case 1** to display the subsection for that test case.

Test Case 1

Summary

Length: 0 Seconds (1 sample periods)
Objective Count: 1

Objectives

Step	Time	Model Item	Objectives
1	0	Multiport Switch	truncated input value = 1 (output is from input port 2)

Generated Parameter Values

Parameter	Value
A	1

Generated Input Data

Time	0
Step	1
In1	-
In2	-

This section provides details about Test Case 1 that the Simulink Design Verifier software generated to satisfy a coverage objective in the model. In this test case, a value of 1 for parameter A satisfies the objective.

- 4** Scroll down to the Test Case 2 section in the **Test Cases** chapter.

Test Case 2

Summary

Length: 0 Seconds (1 sample periods)

Objective Count: 1

Objectives

Step	Time	Model Item	Objectives
1	0	Multiport Switch	truncated input value = 2 (output is from input port 3)

Generated Parameter Values

Parameter	Value
A	2

Generated Input Data

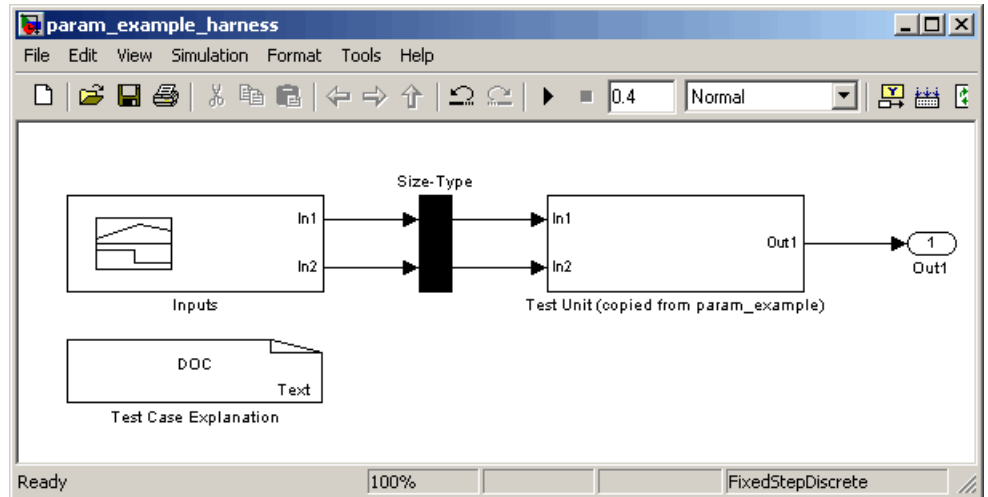
Time	0
Step	1
In1	-
In2	-

This section provides details about Test Case 2, which satisfies another coverage objective in the model. In this test case, a value of 2 for parameter A satisfies the objective.

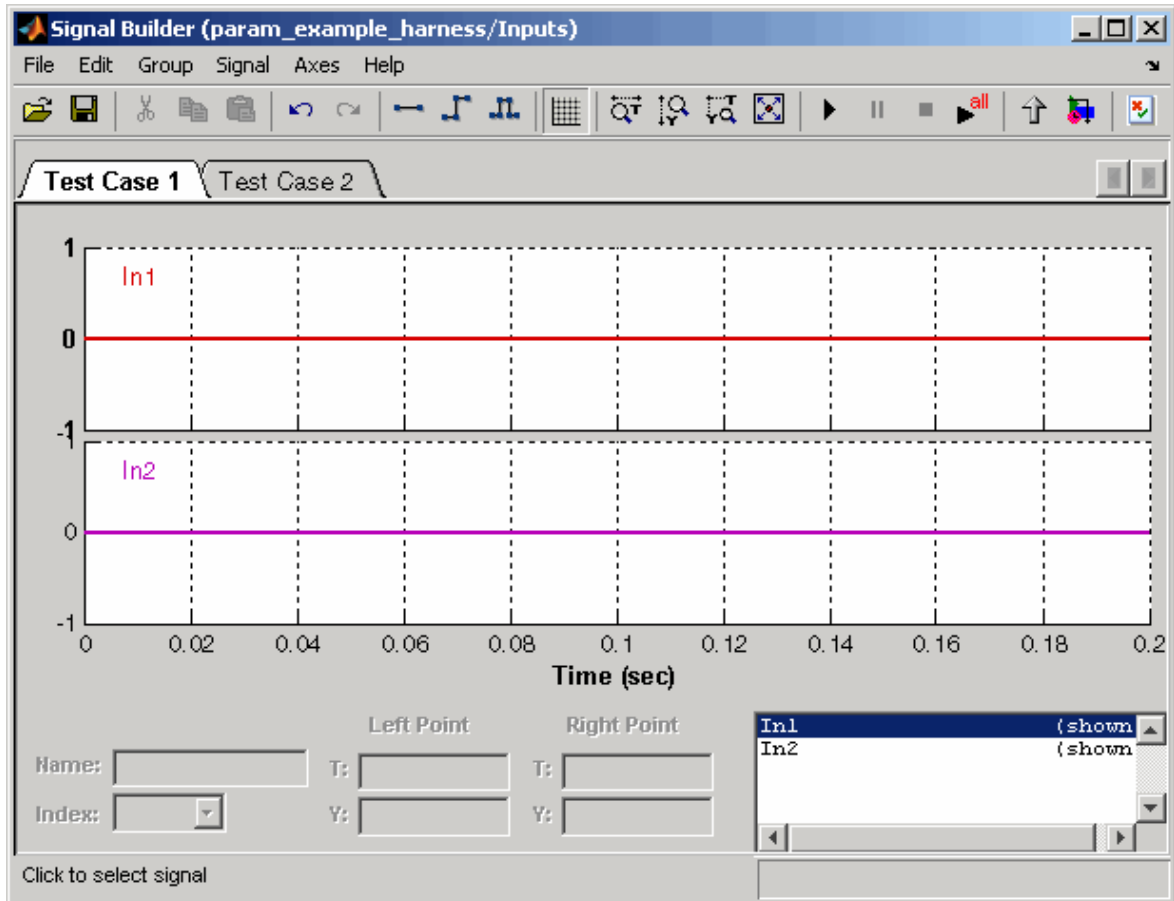
Simulating the Test Cases


In this final task, you simulate the test cases that the Simulink Design Verifier software generated in “Simulating the Test Cases” on page 5-15. In addition, you review the coverage report that results from the simulation.

- 1 Open the test harness model named `param_example_harness.mdl` (if it is not already open).





- 2 The block labeled Inputs in the test harness model is a Signal Builder block that contains the test case signals. Double-click the Inputs block to view the test case signals.



- 3** In the Signal Builder dialog box, click the **Run all** button 

The Simulink software simulates each of the test cases in succession, collects coverage data for each simulation, and displays an HTML report of the combined coverage results at the end of the last simulation.

- 4** In the model coverage report, review the **Summary** section:

Summary	
Model Hierarchy/Complexity:	Test 1
	D1
1. param_example_harness1	2 100% 
2. . . . Test Unit (copied from param_example)	1 100% 

This section summarizes the coverage results for the harness model and its Test Unit subsystem. Observe that the subsystem achieves 100% decision coverage.

5 In the **Summary** section, click the Test Unit subsystem.

The report displays detailed coverage results for the Test Unit subsystem.

2. Subsystem "[Test Unit \(copied from param_example\)](#)"

Parent: [/param_example_harness1](#)

Metric	Coverage (this object)	Coverage (inc. descendants)
Cyclomatic Complexity	0	1
Decision (D1)	NA	100% (2/2) decision outcomes

MultiPortSwitch block "[Multiport Switch](#)"

Parent: [param_example_harness1/Test Unit \(copied from param_example\)](#)

Metric	Coverage
Cyclomatic Complexity	1
Decision (D1)	100% (2/2) decision outcomes

Decisions analyzed:

truncated input value	100%
= 1 (output is from input port 2)	2/4
= 2 (output is from input port 3)	2/4

This section reveals that the Multiport Switch block achieves complete decision coverage because the test cases exercise each of its switch pathways.

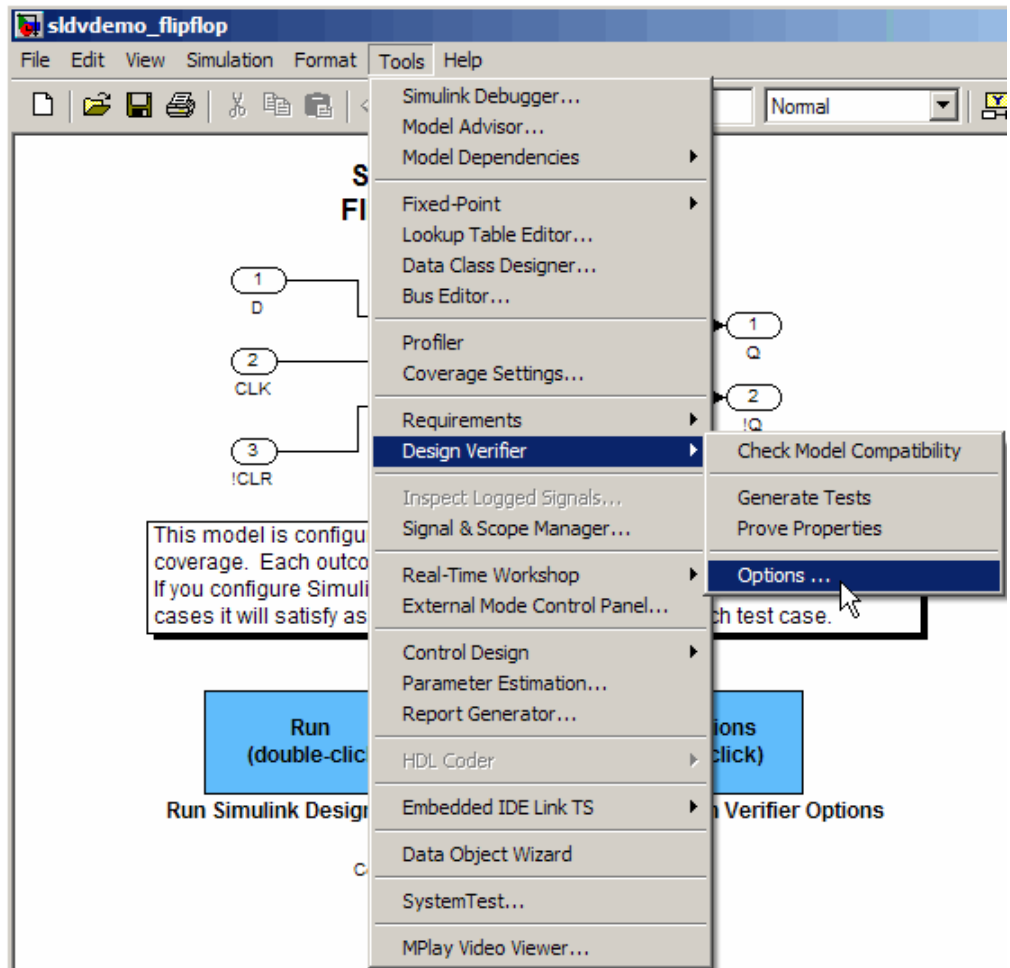
Configuring Simulink Design Verifier Options

This chapter provides an overview of the Simulink Design Verifier options that you specify typically with the Configuration Parameters dialog box. The following sections step you through the Simulink Design Verifier dialog panes and describe its options.

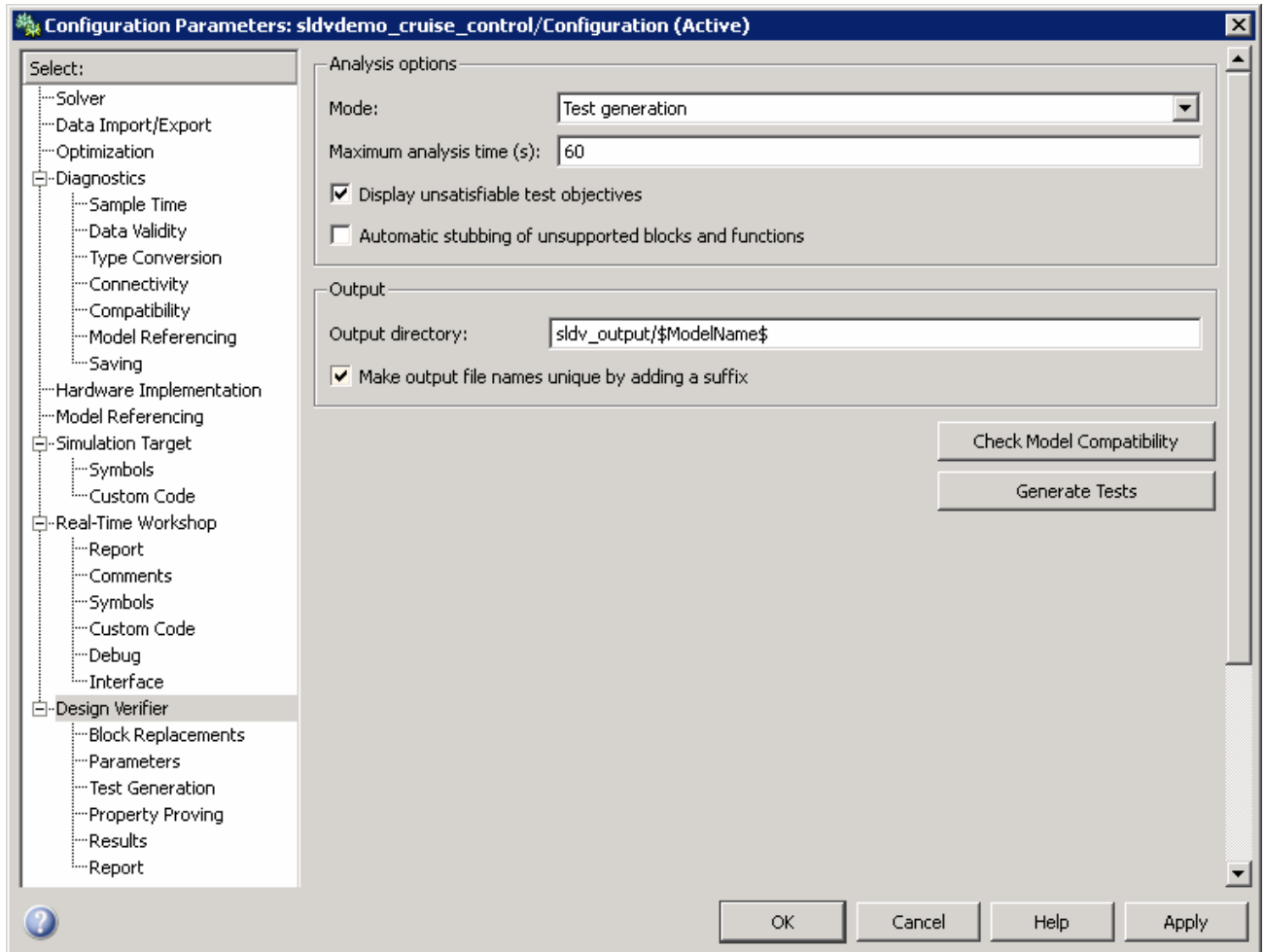
- “Viewing Simulink® Design Verifier Options” on page 6-2
- “Configuring Simulink® Design Verifier Options” on page 6-5
- “Saving Simulink® Design Verifier Options” on page 6-19

Viewing Simulink Design Verifier Options

The Simulink Design Verifier software provides numerous options that control its behavior when analyzing models. To view its options, from the **Tools** menu of your Simulink model, select **Design Verifier > Options**.



The Simulink Design Verifier software displays its options in the Configuration Parameters dialog box.



Typically, you specify values for these options using the Configuration Parameters dialog box. See “Configuration Parameters Dialog Box” in *Simulink Graphical User Interface* for more information about working with this interface.

Note By default, Simulink Design Verifier options do not appear in a model's Configuration Parameters dialog box. If you select **Design Verifier > Options** from a model's **Tools** menu, the Simulink Design Verifier software associates its options with that model. Afterward, you can access those options directly from the Configuration Parameters dialog box or Model Explorer (see “The Model Explorer” in *Simulink User's Guide*).

Alternatively, you can use the `sldvoptions` function to view Simulink Design Verifier options at the command line. Use the following syntax to access and view programmatically the options associated with the Simulink model *system*:

```
opts = sldvoptions('system');  
get(opts)
```

See `sldvoptions` in Chapter 11, “Function Reference” for more information.

Configuring Simulink Design Verifier Options

In this section...

“Design Verifier Pane” on page 6-5
“Block Replacements Pane” on page 6-7
“Parameters Pane” on page 6-9
“Test Generation Pane” on page 6-10
“Property Proving Pane” on page 6-12
“Results Pane” on page 6-14
“Report Pane” on page 6-17

Design Verifier Pane

In the **Design Verifier** pane, you specify analysis options and configure Simulink Design Verifier output.

The screenshot shows the Design Verifier pane with two sections: Analysis options and Output. The Analysis options section includes a Mode dropdown menu set to Test generation, a Maximum analysis time (s) text box containing 600, and two checkboxes: Display unsatisfiable test objectives (checked) and Automatic stubbing of unsupported blocks and functions (unchecked). The Output section includes an Output directory text box containing sldv_output/\$ModelName\$ and a checkbox for Make output file names unique by adding a suffix (checked).

The **Design Verifier** pane contains the following settings:

- “Analysis options” on page 6-6
- “Output” on page 6-6

- “Check Model Compatibility” on page 6-7
- “Generate Tests or Prove Properties” on page 6-7

Analysis options

This group contains the following controls that enable you to specify how the Simulink Design Verifier software analyzes Simulink models.

Mode. Specifies the mode in which the Simulink Design Verifier software operates— **Test generation** (the default) or **Property proving**. Depending on the value of this parameter, if you want to start an analysis, click the **Generate Tests** or **Prove Properties** button on this pane.

Maximum analysis time. Specifies the maximum time (in seconds) that the Simulink Design Verifier software spends analyzing the model. The default value is 600 seconds.

Display unsatisfiable test objectives. If you select this option, it causes the Simulink Design Verifier software to display a warning message in the Simulation Diagnostics Viewer when it cannot satisfy a test objective.

Tip If you first select **Display unsatisfiable test objectives**, set the **Test suite optimization** option to the **Combined objectives** strategy and analyze the model. If that test returns objectives without outcomes, select the **Individual objectives** strategy and reanalyze the model. The **Individual objectives** strategy analyzes each objective independently and more accurately identifies unsatisfiable objectives.

Automatic stubbing of unsupported blocks and functions. If you select this option, it specifies that the Simulink Design Verifier software ignores unsupported blocks and functions, and proceeds with the analysis.

Output

This group contains the following controls that enable you to configure Simulink Design Verifier output.

Output directory. Specifies a directory to which the Simulink Design Verifier software writes its output. Enter a path that is either absolute or relative to the current directory.

The default value is `sldv_output/$modelName$`. `$modelName$` is a token that represents the model name.

Make output file names unique by adding a suffix. If you select this option, it causes the Simulink Design Verifier software to append an incremental numeric suffix to output file names. Selecting this option prevents the software from overwriting existing files that have the same name.

Check Model Compatibility

Click **Check Model Compatibility** to see if your model is compatible with the Simulink Design Verifier software. If you are setting options for a subsystem that you selected, click **Check Subsystem Compatibility**.

Generate Tests or Prove Properties

In the Configuration Parameters dialog box, click **Generate Tests** or **Prove Properties** to analyze a model.

If you set the **Mode** parameter to **Test generation**, click **Generate Tests** to begin a test-case generation analysis of the model. If you are setting options for a subsystem that you selected, click **Generate Tests for Subsystem**.

If you set the **Mode** parameter to **Property proving**, click **Prove Properties** to begin property-proving analysis of the model. If you are setting options for a subsystem that you selected, click **Prove Properties of Subsystem**.

Block Replacements Pane

In the **Block Replacements** pane, you specify options that control how the Simulink Design Verifier software preprocesses the models it analyzes.

The image shows a dialog box titled "Block replacements" with a light gray background. At the top left, the title "Block replacements" is displayed. Below it is a checkbox labeled "Apply block replacements" which is currently unchecked. Underneath the checkbox is the text "List of block replacement rules (in order of priority):" followed by a large, empty rectangular text area. At the bottom of the dialog box, there is a section titled "Output model" containing a text input field labeled "File path of the output model:".

Block replacements

This group contains the following controls that enable you to specify block replacement options.

Apply block replacements. If selected, this option causes the Simulink Design Verifier software to replace blocks in the model before its analysis (see Chapter 4, “Working with Block Replacements”). By default, this option is disabled. Enabling this option provides access to the **List of block replacement rules** and **File path of the output model** options.

List of block replacement rules. Specifies a list of block replacement rules that the Simulink Design Verifier software processes before analyzing the model. This option is accessible only if **Apply block replacements** is selected. The software processes the block replacement rules in the order that you list them.

Specify block replacement rules as a list delimited by spaces, commas, or carriage returns (see “Configuring Block Replacements” on page 4-15).

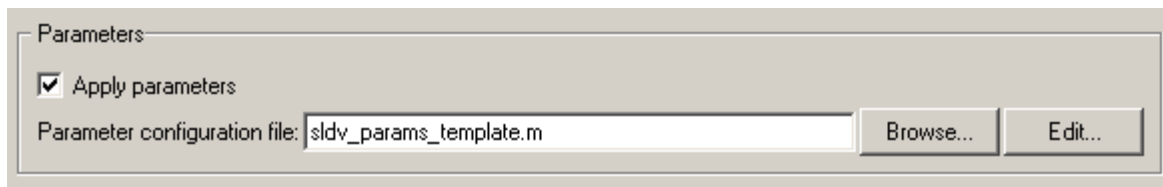
The default value is <FactoryDefaultRules>. If you specify the default value, the Simulink Design Verifier software uses its factory default block replacement rules (see “Built-In Block Replacements” on page 4-3).

File path of the output model. Specifies a directory for the model that results after applying the block replacement rules. Enter a path name that is either absolute or relative to the path name specified as the **Output directory**. This option is accessible only if **Apply block replacements** is selected.

The default value is \$ModelName\$_replacement. \$ModelName\$ is a token that represents the model name.

Parameters Pane

In the **Parameters** pane, you specify options that control how the Simulink Design Verifier software uses parameter configurations when analyzing models.



Parameters

This group contains the following controls that enable you to specify parameter configurations.

Apply parameters. If selected (the default), this option causes the Simulink Design Verifier software to use parameter configurations when analyzing a model (see Chapter 5, “Specifying Parameter Configurations”). Enabling this option provides access to the **Parameter configuration file** option.

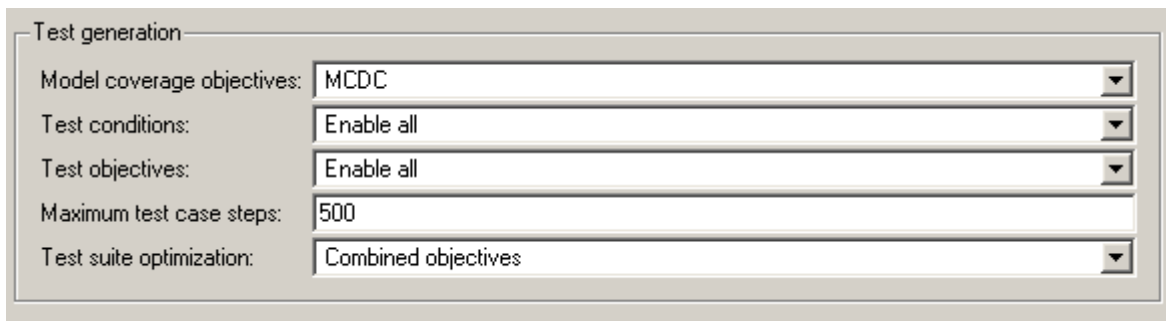
Parameter configuration file. Specifies an M-file function that defines parameter configurations for a model. Click the **Browse** button to select an existing M-file function using a file chooser dialog box. Click the **Edit** button to open the specified M-file function in an editor.

The default value is `sldv_params_template.m`, a template that you can edit and save. The comments in the template explain the syntax you use to specify parameter configurations.

Tip See the Parameter Identification Example demo for an illustration of how to use parameter configurations when generating tests cases for a Simulink model.

Test Generation Pane

In the **Test Generation** pane, you specify options that control how the Simulink Design Verifier software generates tests for the models it analyzes.



The screenshot shows a 'Test generation' pane with the following settings:

Model coverage objectives:	MCDC
Test conditions:	Enable all
Test objectives:	Enable all
Maximum test case steps:	500
Test suite optimization:	Combined objectives

Test generation

This group contains the following controls that enable you to specify test generation options.

Model coverage objectives. Specifies the type of model coverage that the Simulink Design Verifier software attempts to achieve. Select either Decision, Condition Decision, MCDC, or None.

When you set **Model coverage objectives** to MCDC, the Simulink Design Verifier software automatically enables every coverage objective for decision coverage and condition coverage as well. Similarly, enabling coverage for condition coverage causes every decision and condition coverage outcome to be enabled. Each Simulink Design Verifier coverage objective includes all the objectives in a less-strict coverage metric.

Test conditions. This option allows you to enable or disable Test Condition blocks in the current model either globally or locally. Select one of the following options:

- **Use local settings** — Enables or disables Test Condition blocks based on the value of the **Enable** parameter of each block. If a block's **Enable** parameter is selected, the block is enabled; otherwise, the block is disabled.
- **Enable all** — Enables all Test Condition blocks in the model regardless of the settings of their **Enable** parameters.
- **Disable all** — Disables all Test Condition blocks in the model regardless of the settings of their **Enable** parameters.

Test objectives. This option allows you to enable or disable Test Objective blocks in the current model either globally or locally. Select one of the following options:

- **Use local settings** — Enables or disables Test Objective blocks based on the value of the **Enable** parameter of each block. If a block's **Enable** parameter is selected, the block is enabled; otherwise, the block is disabled.
- **Enable all** — Enables all Test Objective blocks in the model regardless of the settings of their **Enable** parameters.
- **Disable all** — Disables all Test Objective blocks in the model regardless of the settings of their **Enable** parameters.

Maximum test case steps. Specifies the maximum number of simulation steps the Simulink Design Verifier software takes when attempting to satisfy a test objective.

Test suite optimization. This option allows you to specify the optimization strategy that the Simulink Design Verifier software uses when generating test cases. Select one of the following options:

- **Combined objectives** — Minimizes the number of test cases in a suite by generating test cases that address more than one test objective. Each test case tends to be long, i.e., it includes many time steps.

This option does not necessarily find unsatisfiable objectives, and often leaves them undecided. To identify unsatisfiable objectives, first, run the

Combined objectives strategy to generate test cases. If the analysis returns objectives without outcomes, set the optimization strategy to **Individual objectives** and rerun the analysis to identify any unsatisfiable objectives.

- **Individual objectives** — Maximizes the number of test cases in a suite by generating test cases that each address only one test objective. Each test case tends to be short, i.e., it includes only a few time steps.

Since each test case is analyzed independently, use this strategy to find unsatisfiable objectives.

- **Large model** — Minimizes the number of test cases in a suite by generating cases that address more than one test objective. This strategy is tailored for large models that contain nonlinearities and numerous test objectives; consequently, it tends to use all the time that the **Maximum analysis time** option allots.
- **Long test cases** — Combines test cases to create a smaller number of test cases. This strategy generates fewer, but longer, test cases that each satisfy multiple test objectives and creates a more efficient analysis and easier-to-review results.

Property Proving Pane

In the **Property Proving** pane, you specify options that control how the Simulink Design Verifier software proves properties for the models it analyzes.



The screenshot shows a 'Property proving' pane with the following settings:

Assertion blocks:	Enable all
Proof assumptions:	Enable all
Strategy:	Find violation
Maximum violation steps:	20

Property proving

This group contains the following controls that enable you to specify property-proving options.

Assertion blocks. This option allows you to enable or disable Assertion blocks in the current model, either globally or locally. Select one of the following options:

- **Use local settings** — Enables or disables Assertion blocks based on the value of the **Enable assertion** parameter of each block. If a block's **Enable assertion** parameter is selected, the block is enabled; otherwise, the block is disabled.
- **Enable all** — Enables all Assertion blocks in the model regardless of the settings of their **Enable assertion** parameters.
- **Disable all** — Disables all Assertion blocks in the model regardless of the settings of their **Enable assertion** parameters.

Proof assumptions. This option allows you to enable or disable Proof Assumption blocks in the current model either globally or locally. Select one of the following options:

- **Use local settings** — Enables or disables Proof Assumption blocks based on the value of the **Enable** parameter of each block. If a block's **Enable** parameter is selected, the block is enabled; otherwise, the block is disabled.
- **Enable all** — Enables all Proof Assumption blocks in the model regardless of the settings of their **Enable** parameters.
- **Disable all** — Disables all Proof Assumption blocks in the model regardless of the settings of their **Enable** parameters.

Strategy. Specifies the strategy the Simulink Design Verifier software uses when proving properties. Select one of the following options:

- **Find violation** — If this strategy is selected, the Simulink Design Verifier software searches for property violations within the number of simulation steps specified by the **Maximum violation steps** option. Enabling this option provides access to the **Maximum violation steps** option.
- **Prove** — If this strategy is selected, the Simulink Design Verifier software performs property proofs.
- **Prove with violation detection** — This strategy combines the **Find violation** and **Prove** strategies. If selected, the Simulink Design Verifier software searches for property violations within the number of simulation

steps specified by the **Maximum violation steps** option; then it attempts to prove properties for which it failed to detect a violation. Enabling this option provides access to the **Maximum violation steps** option.

See “Techniques for Proving Properties of Large Models” on page 10-20.

Maximum violation steps. Specifies the maximum number of simulation steps over which the Simulink Design Verifier software searches for property violations. The software does not search beyond the maximum number of simulation steps that you specify; it does not identify violations that occur later in a simulation. This option is accessible only if **Strategy** specifies either Find violation or Prove with violation detection.

Results Pane

In the **Results** pane, you specify options that control how the Simulink Design Verifier software handles the results that it generates.

The image shows a configuration dialog box with three sections:

- Data file options:**
 - Save test data to file
 - Data file name:
 - Include expected output values
 - Randomize data that do not affect the outcome
- Harness model options:**
 - Save test harness as model
 - Harness model file name:
 - Reference input model in generated harness
- SystemTest options:**
 - Save test harness as SystemTest TEST-file (will reference saved data file)
 - SystemTest file name:

The **Results** pane contains the following groups of options:

- “Data file options” on page 6-15
- “Harness model options” on page 6-16
- “SystemTest options” on page 6-16

Data file options

This group contains the following controls that enable you to specify how the Simulink Design Verifier software handles the MAT-file it produces.

Save test data to file. If selected, this option causes the Simulink Design Verifier software to save the test data it generates to a MAT-file. Enabling this option provides access to the **Data file name** option.

Data file name. Specifies a file name for the MAT-file containing the generated test data. Enter a path name that is either absolute or relative to the directory specified by **Output directory**. This option is accessible only if **Save test data to file** is selected.

The default value is `$ModelName$_sldvdata`. `$ModelName$` is a token that represents the model name.

Include expected output values. If selected, this option causes the Simulink Design Verifier software to simulate the model using the test case signals that it produces. For each test case, the software collects the simulation output values associated with Output blocks in the top-level system and includes those values in the MAT-file that it generates (see “TestCases Field / CounterExamples Field” on page 9-5).

Randomize data that does not affect outcome. If selected, this option causes the Simulink Design Verifier software to assign random values instead of zeros to test case or counterexample signals that have no impact on test or proof objectives in a model. In the Simulink Design Verifier report, the Generated Input Data table always displays a dash (–) for such signals (see “Test Cases / Properties Chapter” on page 9-29).

Harness model options

This group contains the following controls that enable you to specify how the Simulink Design Verifier software handles the test harness it produces.

Save test harness as model. If selected, this option causes the Simulink Design Verifier software to save the test harness it generates as a model file. Enabling this option provides access to the **Harness model file name** option.

Harness model file name. Specifies a file name for the test harness model. Enter a path name that is either absolute or relative to the path name specified by **Output directory**. This option is accessible only if **Save test harness as model** is selected.

The default value is `$modelName$_harness`. `$modelName$` is a token that represents the model name.

Reference input model in generated harness. If selected, this option causes the Simulink Design Verifier software to use model reference to run the input model in the generated test harness instead of inserting a copy of the input model.

SystemTest options

Save test harness as SystemTest TEST-file (will reference saved data file). If selected, this option causes the Simulink Design Verifier software to produce the `.test` configuration file for running generated test cases inside the SystemTest™ environment. Enter a path name that is either absolute or relative to the path name specified by **Output directory**. Enabling this option provides access to the **SystemTest file name** option.

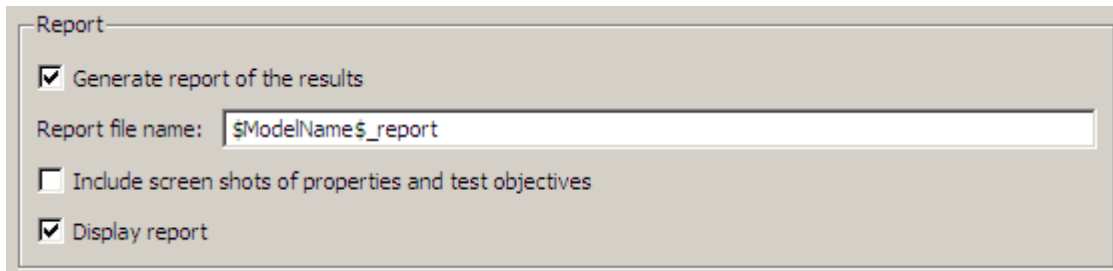
Note The option to create a SystemTest TEST-file is only available in test-generation mode; you cannot create this file when running a property-proving analysis.

SystemTest file name. Specifies a file name for the SystemTest TEST-file. Enter a path name that is either absolute or relative to the path name specified by **Output directory**. This option is accessible only if the **Save test harness as SystemTest TEST-file (will reference saved data file)** is selected.

The default value is \$ModelName\$_harness. \$ModelName\$ is a token that represents the model name.

Report Pane

In the **Report** pane, you specify options that control how the Simulink Design Verifier software reports its results.



Report

Generate report of the results

Report file name:

Include screen shots of properties and test objectives

Display report

Report

This group contains the following controls that enable you to specify report options.

Generate report of the results. If selected, this option causes the Simulink Design Verifier software to save the HTML report it generates. If you select this option, you must also enable the **Save test harness as model** option (see “Harness model options” on page 6-16).

Enabling this option provides access to the **Report file name**, **Include screen shots of properties and test objectives**, and **Display report** options.

Report file name. Specifies a file name for the HTML report. Enter a path name that is either absolute or relative to the directory specified by **Output directory**. This option is accessible only if **Generate report of the results** is selected.

The default value is `$ModelName$_report`. `$ModelName$` is a token that represents the model name.

Include screen shots of properties and test objectives. If selected, this option causes the Simulink Design Verifier software to insert a screen shot of each property to the corresponding section of the HTML report it generates. This option is only valid in property-proving mode. This option is disabled by default. It is accessible only if **Generate report of the results** is selected.

Display report. If selected, this option causes the Simulink Design Verifier software to display the HTML report it generates after completing its analysis. This option is enabled by default. It is accessible only if **Generate report of the results** is selected.

Saving Simulink Design Verifier Options

The Simulink Design Verifier software stores its options as a configuration set component attached to your model file (see “Configuration Sets” in *Simulink User’s Guide*). To save the values of Simulink Design Verifier options that you specified for your model, simply save your model (see “Saving a Model” in *Simulink User’s Guide*).

The Simulink Design Verifier options stay with the model, even if you open the model on a MATLAB installation that does not have a Simulink Design Verifier license. If you then open the model on a system with a Simulink Design Verifier license, the software can analyze the model with the blocks and options that you originally added to the model.

Generating Test Cases

This chapter describes how to use the Simulink Design Verifier software to generate test cases for a model. The following sections introduce the notion of test case generation and present an example in which you generate test cases for a simple Simulink model:

- “About Test Case Generation” on page 7-2
- “Basic Workflow for Generating Test Cases” on page 7-3
- “Generating Test Cases for a Model” on page 7-4
- “Generating Test Cases for a Subsystem” on page 7-30

About Test Case Generation

The Simulink Design Verifier software can generate test cases that satisfy your model's coverage objectives, including:

- Decision coverage
- Condition coverage
- Modified condition/decision coverage (MC/DC)

Test cases assist you in confirming that a model behaves correctly by demonstrating how its blocks execute in different modes. When generating test cases, the software performs a formal analysis of your model. After completing its analysis, the software produces a report that details its results and a test harness model that contains test cases. Simply review the report and simulate the test harness model to confirm that the test cases achieve your model's coverage objectives.

The software provides two blocks that allow you to customize test cases for your Simulink models:

- The Test Objective block defines the values of a signal that a test case must satisfy.
- The Test Condition block constrains the values of a signal during an analysis.

The Simulink Design Verifier software also provides two functions that extend the Stateflow action language, allowing you to customize test cases for your Stateflow charts. These functions behave identically to the Test Objective and Test Condition blocks. Use the following syntax to invoke these functions in a Stateflow chart:

```
dv.test(expr, "{values}")  
dv.condition(expr, "{values}")
```

where `expr` represents the objective or condition, e.g., $x > 0$, and the optional argument `values` specifies the intervals that comprise the test objective or condition. For more information about the `values` argument, see “Specifying Test Objectives” on page 12-18 and “Specifying Test Conditions” on page 12-13.

Basic Workflow for Generating Test Cases

Here is the recommended workflow for generating test cases for your model:

- 1** Ensure that your model is compatible for use with the Simulink Design Verifier software (for an example, see “Checking Compatibility of the Example Model” on page 7-6).
- 2** Optionally, instrument your model with blocks that specify test objectives and test conditions (for an example, see “Customizing Test Generation” on page 7-21).
- 3** Specify Simulink Design Verifier options that control how it generates test cases for your model. (For an example, see “Configuring Test Generation Options” on page 7-10.)
- 4** Execute the Simulink Design Verifier analysis and review its results (for examples, see “Analyzing the Example Model” on page 7-13 and “Reanalyzing the Example Model” on page 7-25).

Generating Test Cases for a Model

In this section...
“About This Example” on page 7-4
“Constructing the Example Model” on page 7-5
“Checking Compatibility of the Example Model” on page 7-6
“Configuring Test Generation Options” on page 7-10
“Analyzing the Example Model” on page 7-13
“Customizing Test Generation” on page 7-21
“Reanalyzing the Example Model” on page 7-25
“Analyzing Contradictory Models” on page 7-29

About This Example

The sections that follow describe a simple Simulink model, for which you generate test cases that achieve decision coverage. This example will help you understand the test-generation capabilities of the Simulink Design Verifier software.

The following workflow guides you through the process of completing this example.

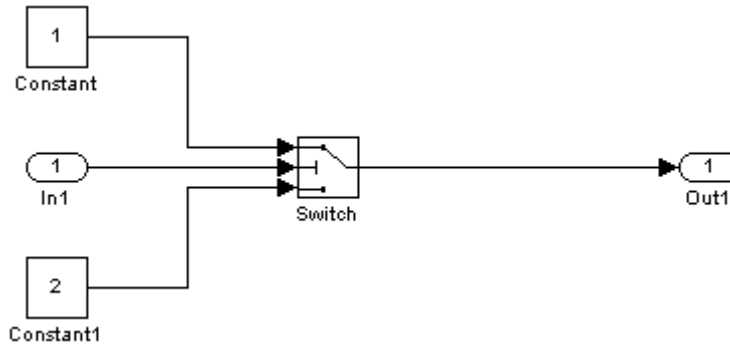
Task	Description	See...
1	Construct the example model.	“Constructing the Example Model” on page 7-5
2	Ensure your model’s compatibility with the Simulink Design Verifier software.	“Checking Compatibility of the Example Model” on page 7-6
3	Configure the Simulink Design Verifier software to generate tests.	“Configuring Test Generation Options” on page 7-10

Task	Description	See...
4	Generate test cases for your model and interpret the results.	“Analyzing the Example Model” on page 7-13
5	Add a Test Condition block to customize test generation.	“Customizing Test Generation” on page 7-21
6	Generate test cases for your modified model and interpret the results.	“Reanalyzing the Example Model” on page 7-25

Constructing the Example Model

In this task, you construct a simple Simulink model that you use throughout the remaining tasks:

- 1 Create a new Simulink model.
- 2 Copy the following blocks into your empty model window:
 - An Inport block, from the Sources library, to initiate the input signal whose value the Simulink Design Verifier software controls
 - A Switch block to provide simple logic, from the Signal Routing library
 - Two Constant blocks to serve as Switch block data inputs, from the Sources library
 - An Outport block to receive the output signal, from the Sinks library
- 3 Double-click one of the Constant blocks in your model and specify its **Constant value** parameter as 2.
- 4 Connect the blocks so that your model appears similar to the following diagram.



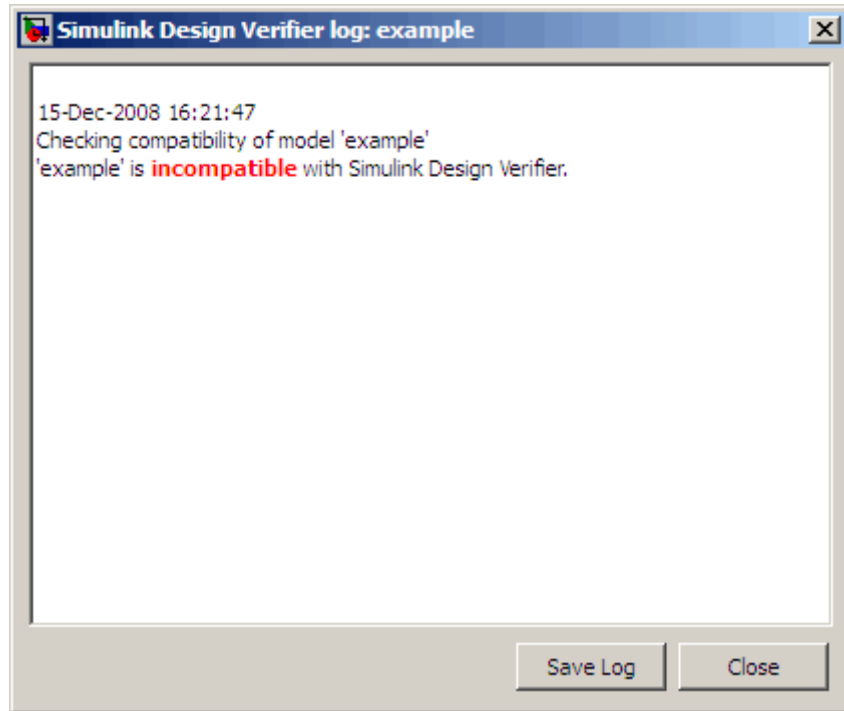
- 5 Save your model as `example.mdl` for use in the remaining tasks.

Checking Compatibility of the Example Model

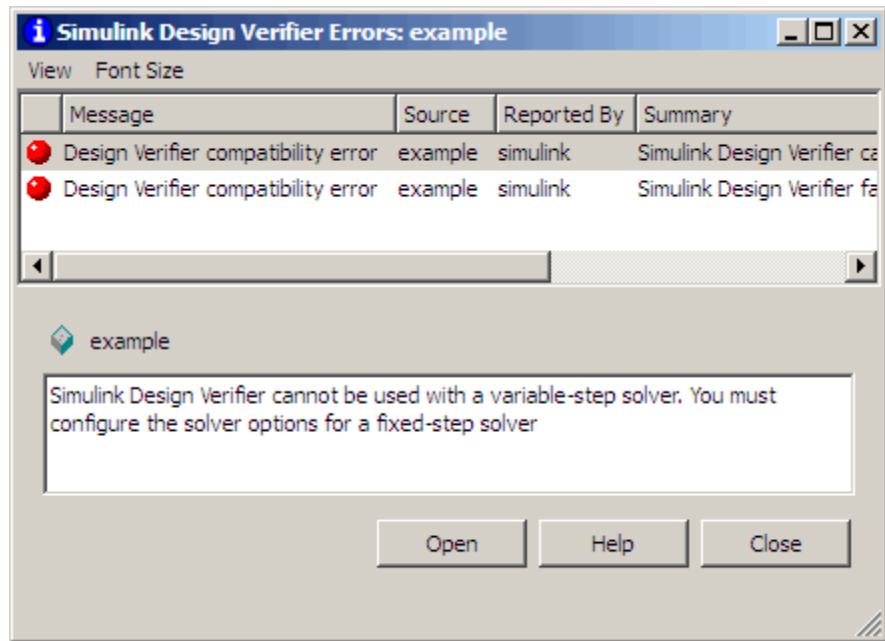
In this task, you ensure that your model is compatible for use with the Simulink Design Verifier software. Specifically, you check the compatibility of the `example` model:

- 1 In your Simulink model window, select **Tools > Design Verifier > Check Model Compatibility**.

The Simulink Design Verifier software displays the following log window, which indicates that your model is incompatible.



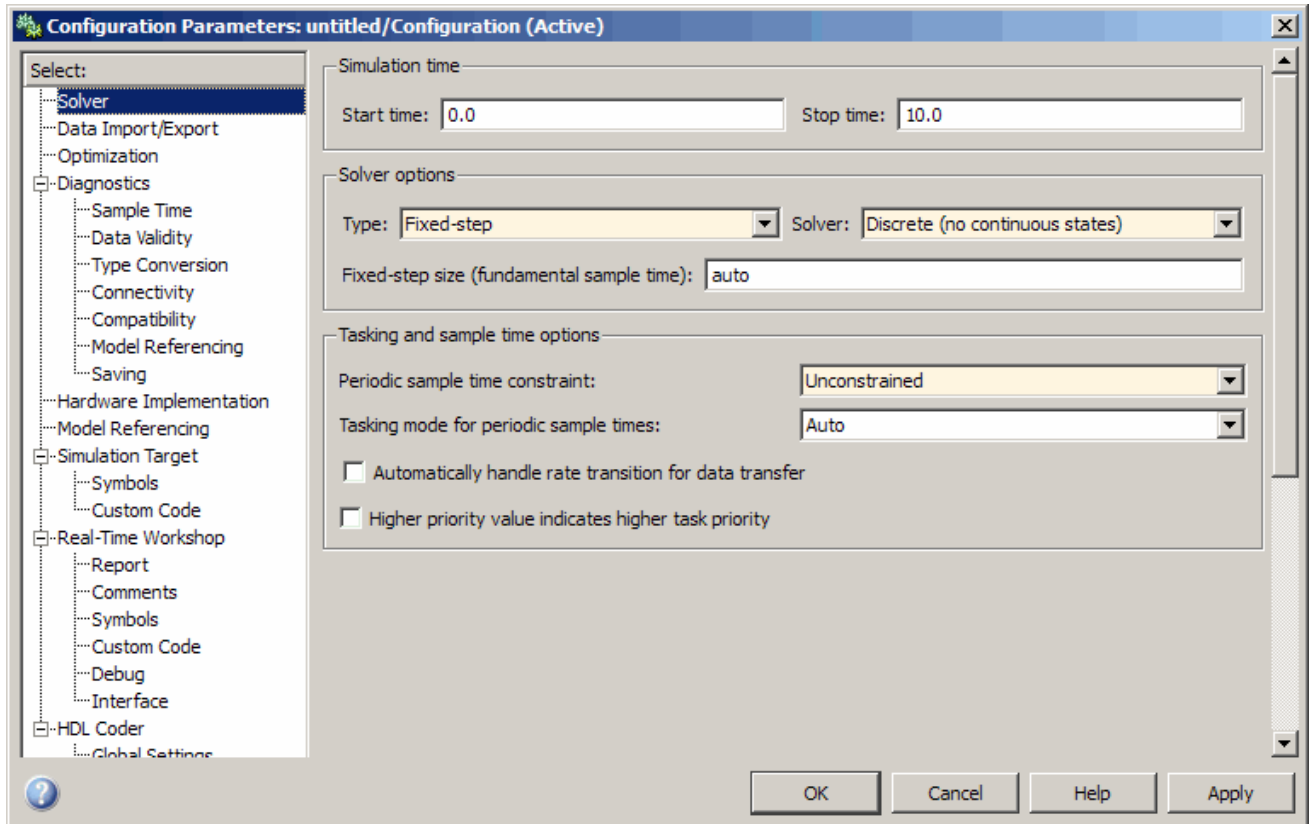
It also displays the following incompatibility error in the Simulation Diagnostics Viewer.



The error message informs you that the Simulink Design Verifier software does not support variable-step solvers. To work around this incompatibility, you must use a fixed-step solver.

- 2 In your Simulink model window, select **Simulation > Configuration Parameters** to display the Configuration Parameters dialog box.
- 3 In the **Select** tree on the left side of the Configuration Parameters dialog box, click the **Solver** category (if not already selected). Under **Solver options** on the right side, set the **Type** option to **Fixed-step** and set the **Solver** option to **Discrete** (no continuous states).

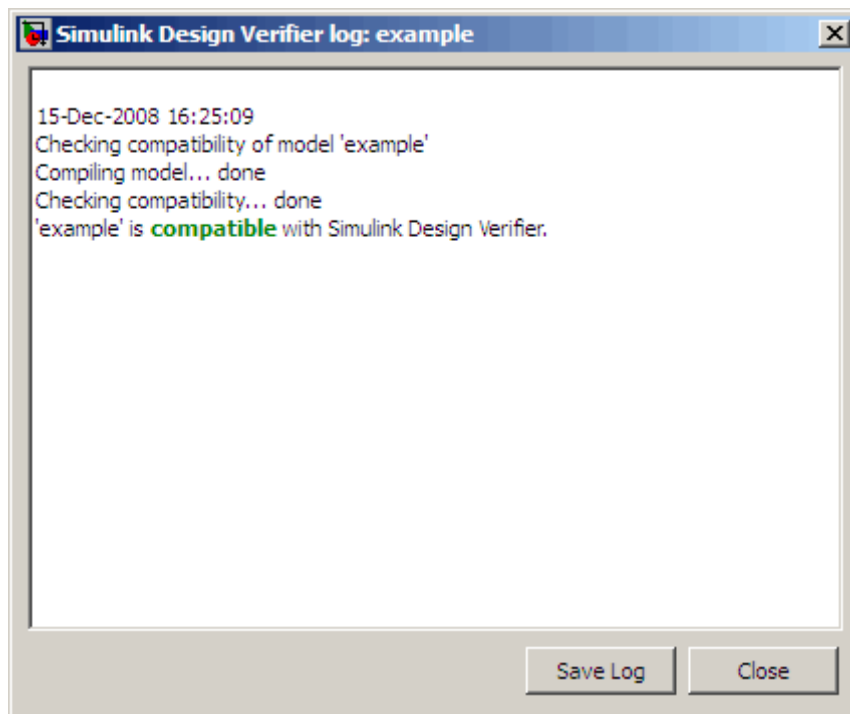
The Configuration Parameters dialog box should look like this.



4 Click **Apply** and **OK** to apply your changes and close the Configuration Parameters dialog box.

5 Recheck the compatibility of your model. In your Simulink model window, select **Tools > Design Verifier > Check Model Compatibility**.

The Simulink Design Verifier software displays the following log window, which confirms that your model is compatible for analysis.



6 Save your model for use in the next task.

What If a Model Is Partially Compatible?

If the compatibility check indicates that your model is partially compatible, your model contains at least one element that is incompatible with the Simulink Design Verifier software. You can continue analyzing a partially compatible model if you turn on automatic stubbing. For details, see “Handling Incompatibilities with Automatic Stubbing” on page 2-6.

Configuring Test Generation Options

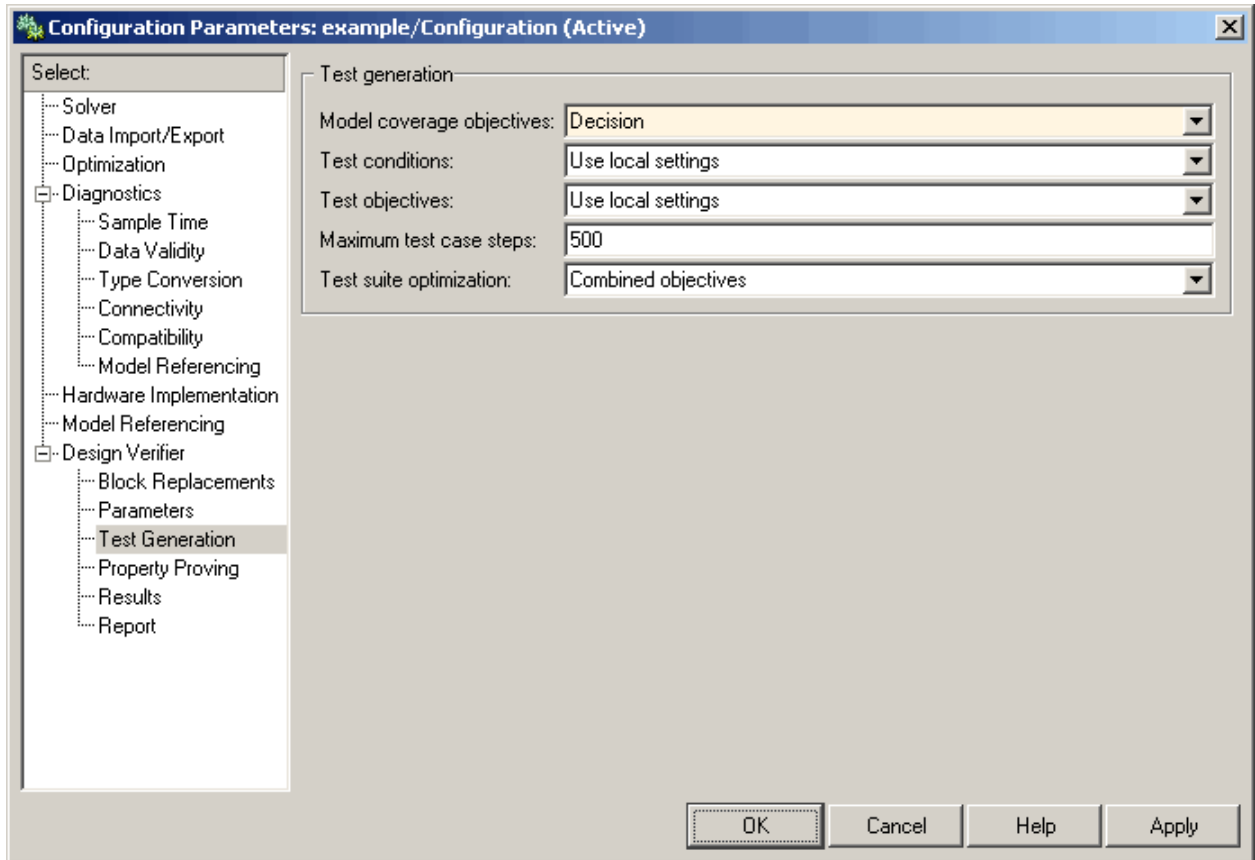
In this task, you configure the Simulink Design Verifier software to generate test cases that achieve complete decision coverage for your simple model:

1 In your Simulink model window, select **Tools > Design Verifier > Options**.

The Simulink Design Verifier options appear in the Configuration Parameters dialog box.

- 2** In the **Select** tree on the left side of the Configuration Parameters dialog box, click the **Design Verifier** category (if not already selected). Under **Analysis options** on the right side, ensure that the **Mode** option specifies **Test generation**.
- 3** In the **Select** tree on the left side of the Configuration Parameters dialog box, click the **Test Generation** category.
- 4** On the **Test Generation** pane, set the value of the **Model coverage objectives** parameter to **Decision**.

The Configuration Parameters dialog box appears as follows.



Note The **Test suite optimization** parameter is set by default to Combined objectives. If you want to generate fewer but longer test cases, select Long test cases for the **Test suite optimization** parameter.

- 5 Click **Apply** and **OK** to apply your change and close the Configuration Parameters dialog box.
- 6 Save your model for use in the next task.

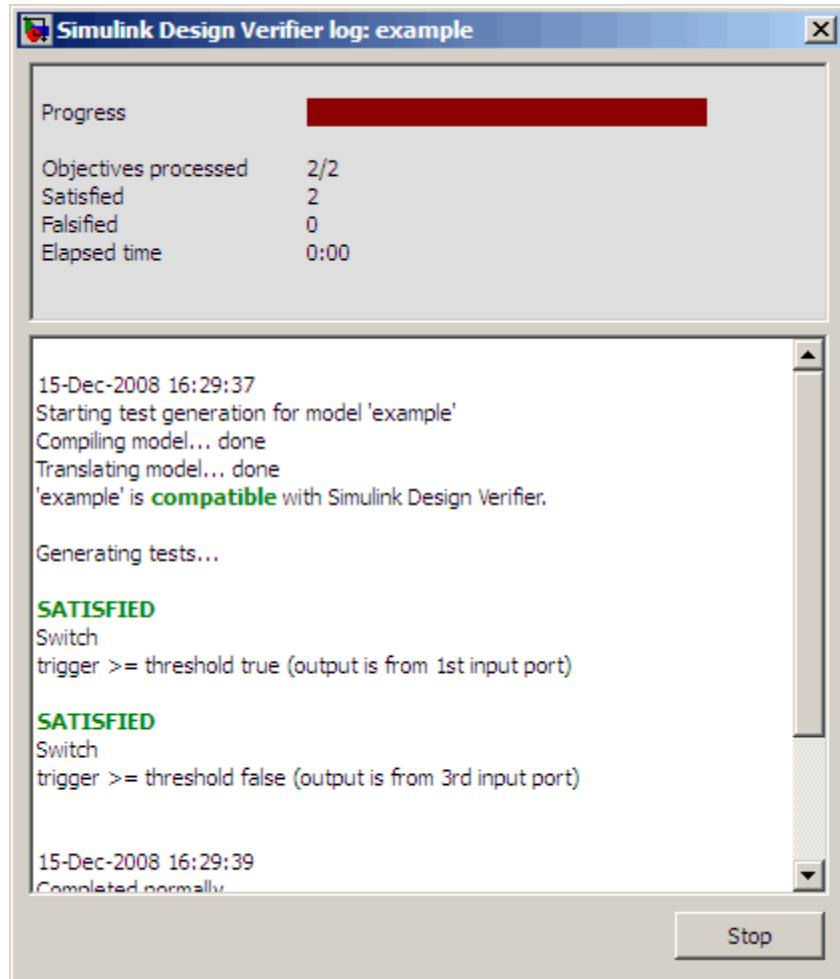
Note On the **Test Generation** pane, you can optionally specify values for other parameters that control how the Simulink Design Verifier software generates test cases for your model. See “Test Generation Pane” on page 6-10 for more information.

Analyzing the Example Model

In this task, you execute the Simulink Design Verifier analysis you configured in the previous task. The software generates test cases for your example model and produces results for you to interpret:

- 1 In your model window, select **Tools > Design Verifier > Generate Tests**.

The Simulink Design Verifier software begins analyzing your model to generate test cases. During its analysis, the software displays a log window.



The log window updates you on the progress of the analysis, providing information such as the number of test objectives processed and how many of those objectives were satisfied. The log window includes a **Stop** button that you can click to terminate the proof at any time.

When the software completes its analysis, it displays the following items:

- An HTML report named `example_report.html`

- A test harness model named `example_harness.mdl`
- A Signal Builder window containing the test-case signals

The remaining steps in this section help you interpret the results that you obtained.

- 2 Review the Simulink Design Verifier report, starting with the **Table of Contents**, whose items you can click to navigate the report.

Table of Contents
1. Summary
2. Analysis Information
3. Test Objectives Status
4. Model Items
5. Test Cases

- 3 In the **Table of Contents**, click Summary to display the report's Summary chapter.

Chapter 1. Summary	
Analysis Information	
Model:	example
Mode:	TestGeneration
Status:	Completed normally
Objectives Status	
Number of Objectives:	2
Objectives Satisfied:	2

The Summary chapter lists information about the model and the status of the objectives—satisfied or not.

- 4 In the **Table of Contents**, click Analysis Information to display the report's Analysis Information chapter.

Chapter 2. Analysis Information

Table of Contents

[Model Information](#)
[Analysis Options](#)
[Approximations](#)

Model Information

File: C:\SLVNN\example.mdl
 Version: 1.2
 Time Stamp: Mon Dec 15 16:28:43 2008
 Author: slemaire

Analysis Options

Mode: TestGeneration
 Test Suite Optimization: CombinedObjectives
 Maximum Testcase Steps: 500 time steps
 Test Conditions: UseLocalSettings
 Test Objectives: UseLocalSettings
 Model Coverage Objectives: Decision
 Maximum Processing Time: 600s
 Block Replacement: off
 Parameters Analysis: off
 Save Data: on
 Save Harness: on
 Save Report: on

Approximations

Simulink Design Verifier performed the following approximations during analysis. These can impact the precision of the results generated by Simulink Design Verifier. Please see the product documentation for further details.

 	Type	Description
1	Rational approximation	The model includes floating-point arithmetic. Simulink Design Verifier approximates floating-point arithmetic with rational number arithmetic.

The Analysis Information chapter provides information about:

- The model you analyzed
- The options you specified for the analysis
- Approximations the software performed during the analysis

- 5 In the **Table of Contents**, click **Test Objectives Status** to display the report's Test Objectives Status chapter.

Chapter 3. Test Objectives Status

Table of Contents

[Objectives Satisfied](#)

Objectives Satisfied

Simulink Design Verifier found test cases that exercise these test objectives.

#:	Type	Model Item	Description	Test Case
1	Decision	Switch	trigger >= threshold false (output is from 3rd input port)	2
2	Decision	Switch	trigger >= threshold true (output is from 1st input port)	1

This table indicates that the software satisfied both test objectives associated with the Switch block in your model, for which it generated two test cases.

- 6 Under the **Test Case** column of the table, click 2 to display the report's Test Case 2 section.

Test Case 2

Summary

Length: 0 Seconds (1 sample periods)
Objective Count: 1

Objectives

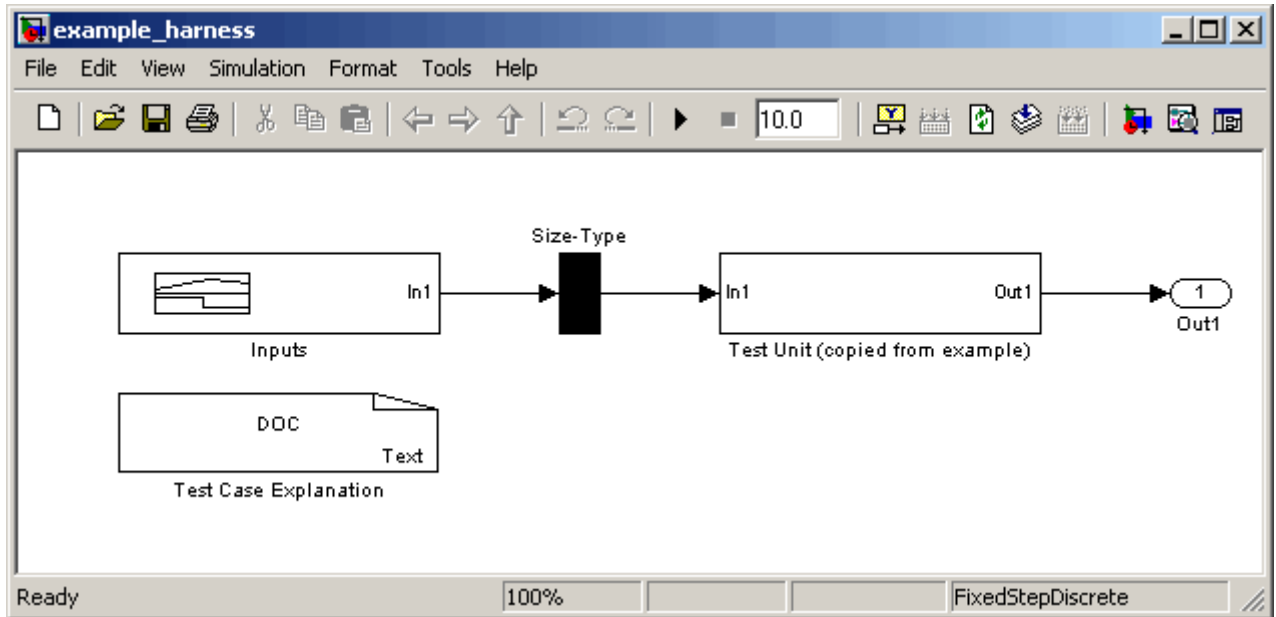
Step	Time	Model Item	Objectives
1	0	Switch	trigger >= threshold false (output is from 3rd input port)

Generated Input Data

Time	0
Step	1
In1	-1

This section provides details about a test case that the Simulink Design Verifier software generated to achieve an objective in your model. This test case achieves test objective 1, which involves the Switch block passing its third input. Specifically, the software determined that a value of -1 for the Switch block control signal enables the block to pass its third input.

- 7** Review the harness model named `example_harness.mdl`.

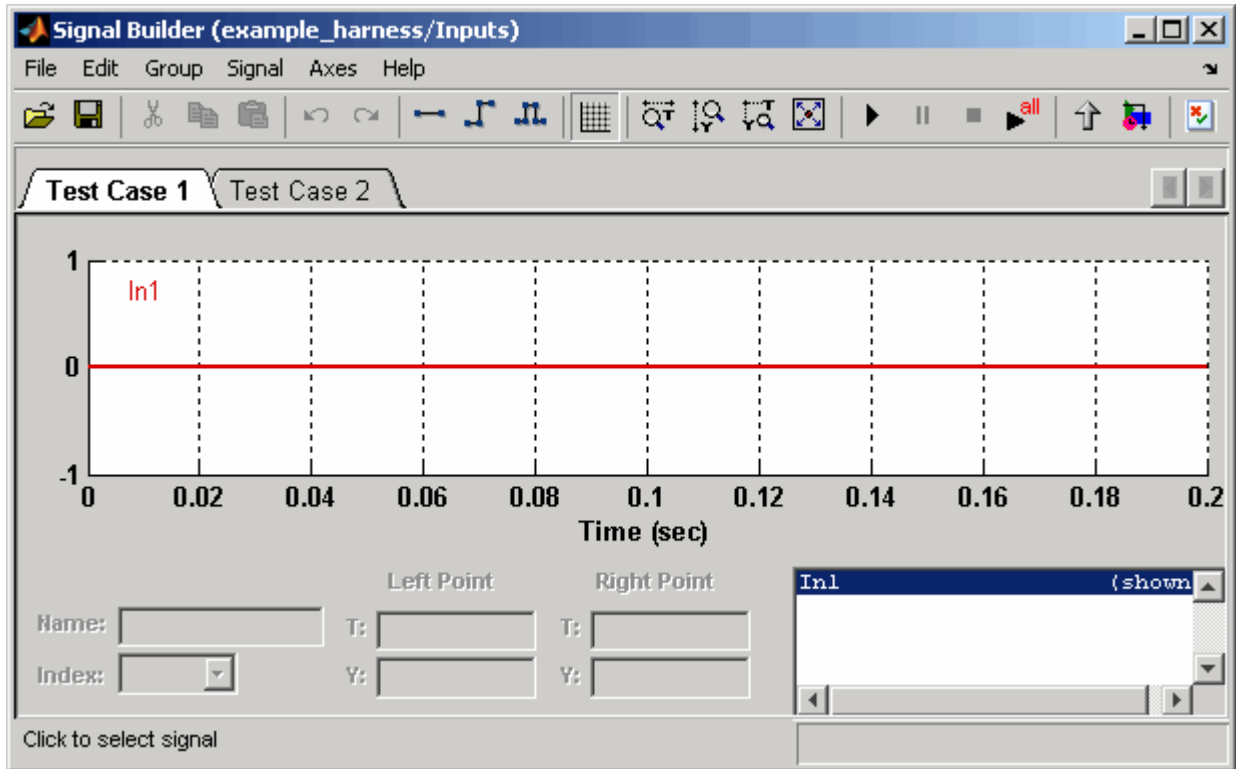



The harness model contains the following items:

- Signal Builder block named **Inputs** — Groups of signals that achieve test objectives in your model
- Subsystem block named **Test Unit** — A copy of your model
- DocBlock named **Test Case Explanation** — A text description of the test cases that the Simulink Design Verifier software generates

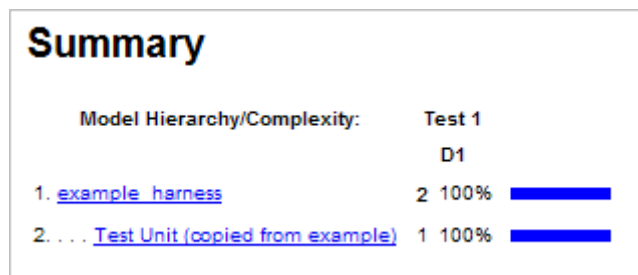
Note See the *Simulink Reference* for more information about interacting with blocks such as the Signal Builder, Subsystem, and DocBlock.

- 8 To simulate the test harness and confirm that the test cases achieve complete decision coverage, double-click the Inputs block to display the Signal Builder dialog box.



- 9 In the Signal Builder dialog box, click the **Run all** button 

The Simulink Design Verifier software simulates the test harness using all the test cases, collects model coverage information, and displays a coverage report that includes the following Summary.



The coverage report indicates that the software generated test cases that achieve complete decision coverage for your example model (see “Understanding Model Coverage Reports” in the *Simulink Verification and Validation User’s Guide*).

What If the Analysis Generates Many Test Cases?

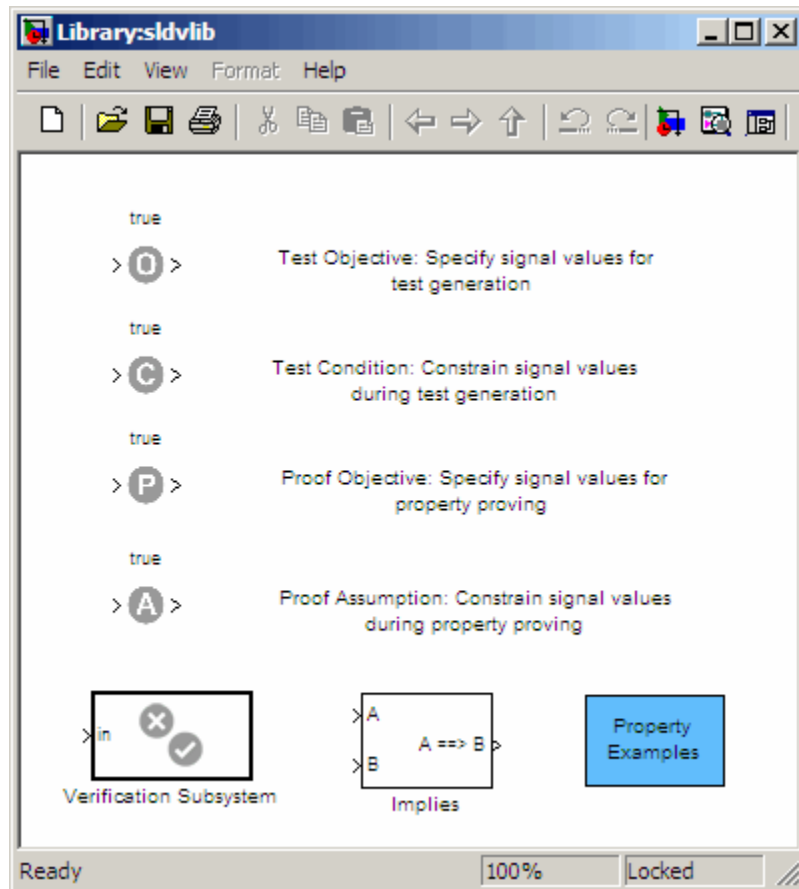
If you prefer to review results that are combined into a smaller number of longer test cases, set the **Test suite optimization** parameter to **Long test cases** and rerun the analysis. In the **Long test cases** optimization, the analysis generates fewer but longer test cases that each satisfy multiple test objectives. This optimization creates a more efficient analysis and easier-to-review results.

To compare the **Long test cases** results to the **Combined objectives** results (the default), see “Combining Test Cases” on page 1-23.

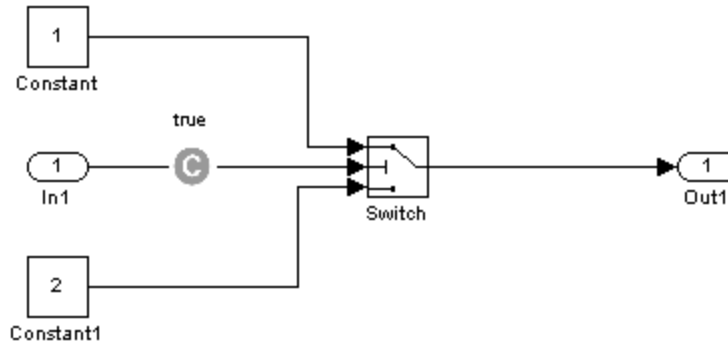
Customizing Test Generation

In this task, you modify the example model for which you attained complete decision coverage. Specifically, you customize test generation by adding and configuring a Test Condition block:

- 1 In the MATLAB Command Window, enter `sldvlib` to display the Simulink Design Verifier library.



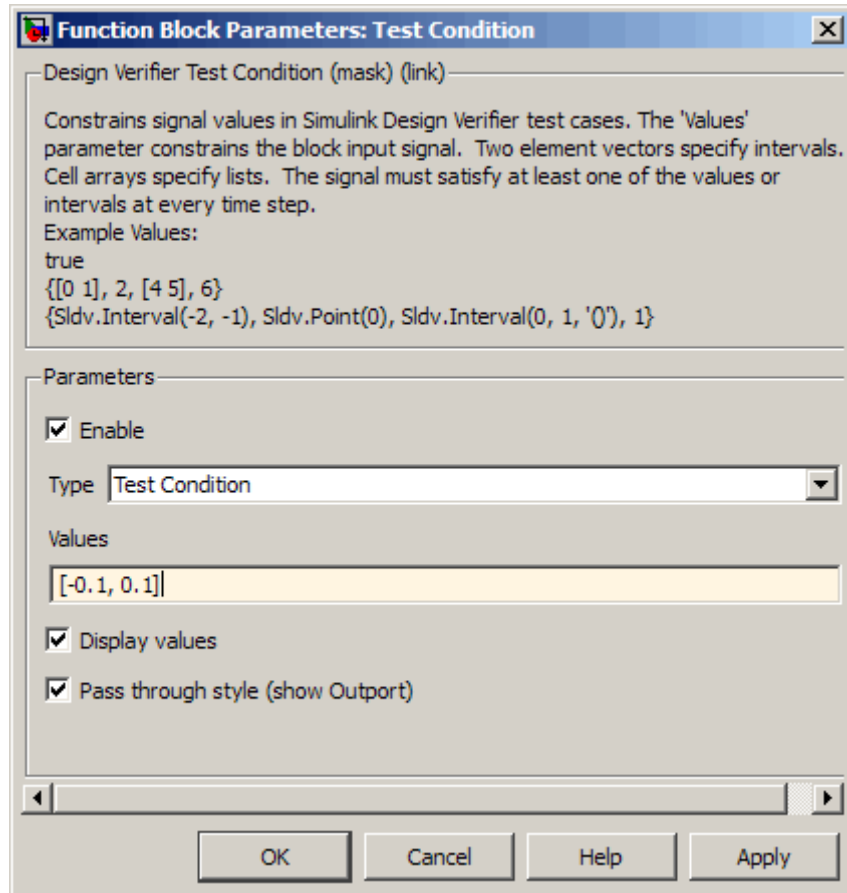
- 2 Copy the Test Condition block to your model by dragging it from the Simulink Design Verifier library to your model window.
- 3 In the model window, insert the Test Condition block between the Switch and Outport blocks.



- 4 Double-click the Test Condition block in your model to access its attributes.

The Test Condition block parameter dialog box appears.

- 5 In the **Values** box, enter $[-0.1, 0.1]$. When generating test cases for this model, the Simulink Design Verifier software constrains the signal values entering the Switch block control port to the specified interval.



6 Click **OK** to apply your changes and close the Test Condition block parameter dialog box.

7 Save your model for use in the next task.

Simulink Design Verifier blocks are preserved with a model, even if you open the model on a MATLAB installation that does not have a Simulink Design Verifier license. If you then open the model on a system with a Simulink Design Verifier license, the software can analyze the model with the blocks and options that you originally added to the model.

Reanalyzing the Example Model

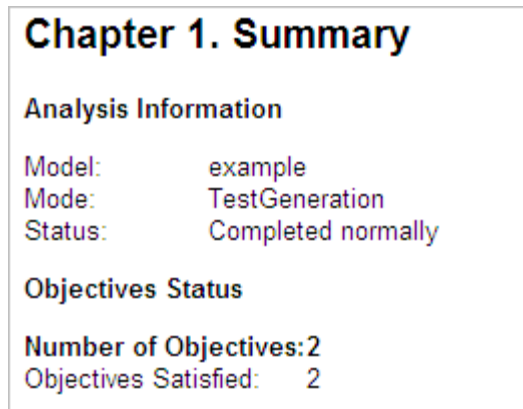
In this task, you analyze the example model with the Test Condition block. To observe how the Test Condition block affects test generation, compare the result of this analysis to the result that you obtained in “Analyzing the Example Model” on page 7-13.

- 1 In the model window, select **Tools > Design Verifier > Generate Tests**.

The Simulink Design Verifier software displays a log window and begins analyzing your model to generate test cases.

When the software completes the analysis, it displays a new Simulink Design Verifier report named `example_report1.html`.

- 2 To begin reviewing the report, in the **Table of Contents**, click **Summary**.



Chapter 1. Summary

Analysis Information

Model: example
Mode: TestGeneration
Status: Completed normally

Objectives Status

Number of Objectives: 2
Objectives Satisfied: 2

The Summary chapter indicates that the Simulink Design Verifier software satisfied two test objectives in your model.

- 3 In the **Table of Contents**, click **Analysis Information**. Scroll to the bottom of this chapter, to the **Constraints** section.

Constraints	
Name	Constraint
Test Condition	[-0.1, 0.1]

This section lists the Test Condition block that you added to constrain the value of the Switch block control signal to the interval [-0.1, 0.1].

- 4** In the **Table of Contents**, click **Test Objectives Status**.

Chapter 3. Test Objectives Status

Table of Contents

[Objectives Satisfied](#)

Objectives Satisfied

Simulink Design Verifier found test cases that exercise these test objectives.

#:	Type	Model Item	Description	Test Case
1	Decision	Switch	trigger >= threshold false (output is from 3rd input port)	2
2	Decision	Switch	trigger >= threshold true (output is from 1st input port)	1

This table indicates that the Simulink Design Verifier software satisfied both test objectives associated with the Switch block in your model, for which it generated two test cases.

- 5** Under the **Test Cases** column of the table, click **2**.

Test Case 2

Summary

Length: 0 Seconds (1 sample periods)
Objective Count: 1

Objectives

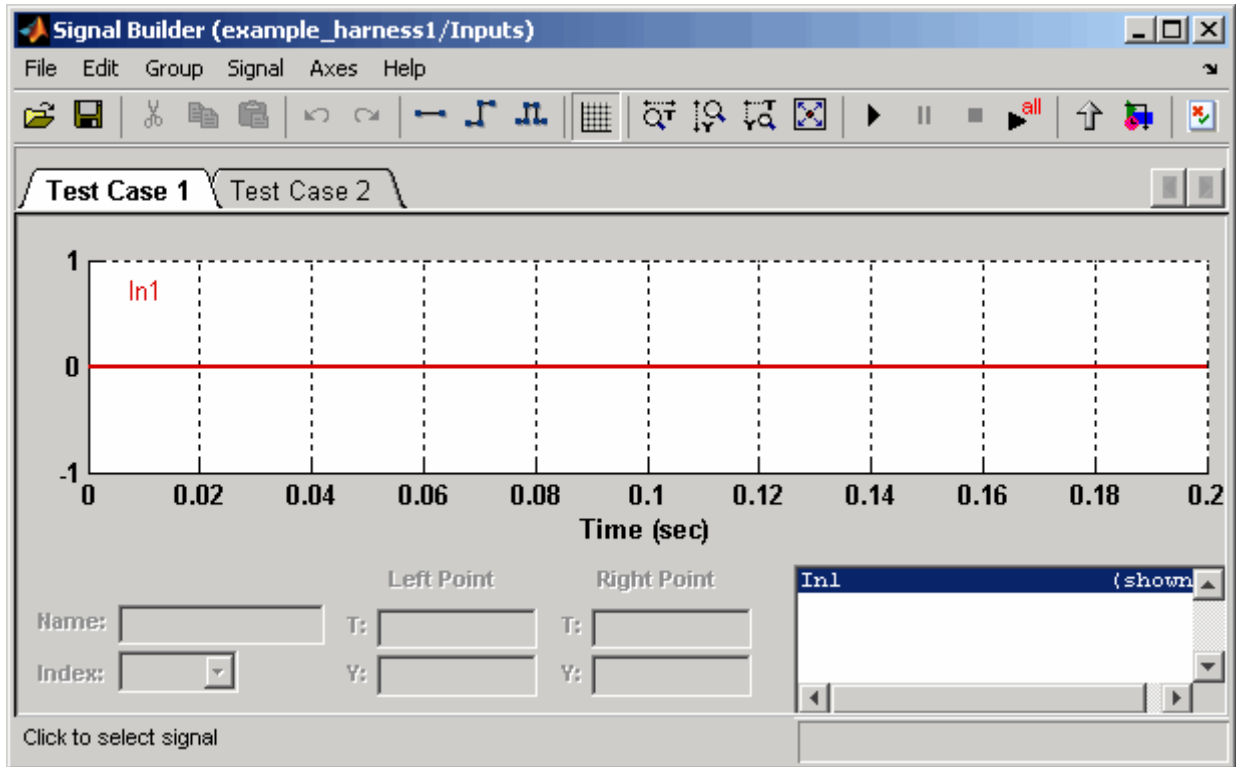
Step	Time	Model Item	Objectives
1	0	Switch	trigger \geq threshold false (output is from 3rd input port)


Generated Input Data

Time	0
Step	1
In1	-0.05

This section provides details about a test case that the software generated to achieve an objective in your model. This test case achieves test objective 1, which involves the Switch block passing its third input. Although the Test Condition block restricted the domain of input signals to the interval $[-0.1, 0.1]$, the software determined that a value of -0.05 for the Switch block control signal satisfies the objective.

- 6 To confirm that the test case achieves complete decision coverage, go to the harness model named `example_harness1.mdl`.
- 7 Double-click the Inputs block to display the Signal Builder dialog box.



- 8 In the Signal Builder dialog box, click the **Run all** button 

The Simulink software simulates the test harness using both test cases, collects model coverage information, and displays a coverage report whose Summary section appears as follows.

Summary		
Model Hierarchy/Complexity:	Test 1	
	D1	
1. example_harness1	3	100% 
2. ... Test Unit (copied from example)	2	100% 

The coverage report indicates the Simulink Design Verifier software generated test cases that achieve complete decision coverage for your example model.

Analyzing Contradictory Models

If the analysis produces the error `The model is contradictory in its current configuration`, the software detected a contradiction in your model and it cannot analyze the model. You can have a contradiction if your model has Test Objective blocks with incorrect parameters, for example, an objective that states that a signal has to be between 0 and 5 when the signal is constant 10.

If the software detects a contradiction, all previous results are invalidated and the software reports that the some of the objectives are unsatisfiable.

Generating Test Cases for a Subsystem

If you have a large model, you can generate test cases for subsystems in the model and review the analysis in smaller, manageable reports. The workflow for generating test cases for a subsystem is as follows:

- 1 Open the model that contains the subsystem.
- 2 Make the subsystem atomic.
- 3 Run the Simulink Design Verifier software using the **Generate Tests for Subsystem** option.
- 4 Review the results.

The tutorial in “Analyzing a Subsystem” on page 1-26 explains how to analyze the Controller subsystem in the Cruise Control Test Generation model.

Proving Properties of a Model

This chapter describes how to use the Simulink Design Verifier software to prove properties of your model. The following sections introduce the notion of property proofs and present an example in which you prove a property of a simple Simulink model:

- “About Property Proofs” on page 8-2
- “Basic Workflow for Proving Model Properties” on page 8-3
- “Proving Properties in a Model” on page 8-4
- “Proving Properties in a Subsystem” on page 8-27
- “Proving Complex Properties” on page 8-28

About Property Proofs

The Simulink Design Verifier software can prove properties of your model. Here, the term *property* refers to a logical expression of signal values in a model. For example, you can specify that a signal in your model should attain a particular value or range of values during simulation. You can then use the Simulink Design Verifier software to prove whether such properties are valid. The software performs a formal analysis of your model to prove or disprove the specified properties. If the software disproves a property, it provides a counterexample that demonstrates a property violation.

The Simulink Design Verifier software provides two blocks that allow you to specify properties in your Simulink models. Use the Proof Objective block to define the values of a signal that the Simulink Design Verifier software will prove. Use the Proof Assumption block to constrain the values of a signal during a proof. For more information about these blocks, refer to Chapter 12, “Block Reference”.

Note Blocks from the Model Verification library in the Simulink software behave like a Proof Objective block during Simulink Design Verifier proofs. Hence, you can use Assertion blocks and other Model Verification blocks to specify properties of your model. See “Model Verification” in the *Simulink Reference* for more information about these blocks.

The Simulink Design Verifier software also provides two functions that extend the Stateflow action language, allowing you to specify properties in your Stateflow charts. These functions behave identically to the Proof Objective and Proof Assumption blocks. Use the following syntax to invoke these functions in a Stateflow chart:

```
dv.prove(expr, "{values}")  
dv.assume(expr, "{values}")
```

where `expr` represents the objective or assumption, e.g., $x > 0$, and the optional argument `values` specifies the intervals that comprise the proof objective or assumption. For more information about the `values` argument, see “Specifying Proof Objectives” on page 12-8 and “Specifying Proof Assumptions” on page 12-3.

Basic Workflow for Proving Model Properties

Here is the recommended workflow for proving properties of your model:

- 1** Ensure that your model is compatible for use with the Simulink Design Verifier software (for an example, see “Checking Compatibility of the Example Model” on page 8-6).
- 2** Instrument your model with blocks that specify proof objectives and proof assumptions (for examples, see “Instrumenting the Example Model” on page 8-10 and “Customizing the Example Proof” on page 8-21).
- 3** Specify Simulink Design Verifier options that control how it proves the properties of your model (for an example, see “Configuring Property-Proving Options” on page 8-13).
- 4** Execute the Simulink Design Verifier analysis and review its results (for examples, see “Analyzing the Example Model” on page 8-15 and “Reanalyzing the Example Model” on page 8-24).

See “Proving Properties in a Model” on page 8-4 for an exercise that demonstrates this workflow.

Proving Properties in a Model

In this section...
“About This Example” on page 8-4
“Constructing the Example Model” on page 8-5
“Checking Compatibility of the Example Model” on page 8-6
“Instrumenting the Example Model” on page 8-10
“Configuring Property-Proving Options” on page 8-13
“Analyzing the Example Model” on page 8-15
“Customizing the Example Proof” on page 8-21
“Reanalyzing the Example Model” on page 8-24
“Analyzing Contradictory Models” on page 8-25

About This Example

The sections that follow describe a simple Simulink model, for which you prove a property that you specify using a Proof Objective block. This example will help you understand the property-proving capabilities of the Simulink Design Verifier software.

The following workflow guides you through the process of completing this example:

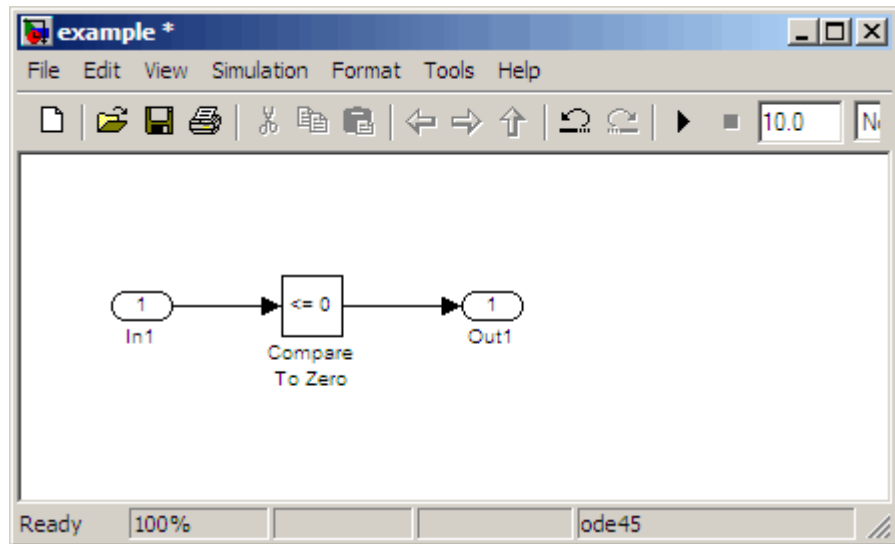
Task	Description	See...
1	Construct the example model.	“Constructing the Example Model” on page 8-5
2	Ensure your model’s compatibility with the Simulink Design Verifier software.	“Checking Compatibility of the Example Model” on page 8-6
3	Add a Proof Objective block to your model to prepare for its proof.	“Instrumenting the Example Model” on page 8-10

Task	Description	See...
4	Configure the Simulink Design Verifier software to prove properties.	“Configuring Property-Proving Options” on page 8-13
5	Prove a property of your model and interpret the results.	“Analyzing the Example Model” on page 8-15
6	Add a Proof Assumption block to customize the proof.	“Customizing the Example Proof” on page 8-21
7	Prove a property of your modified model and interpret the results.	“Reanalyzing the Example Model” on page 8-24

Constructing the Example Model

In this task, you construct a simple Simulink model that you use throughout the remaining tasks. To complete this task, perform the following steps:

- 1** Create an empty Simulink model.
- 2** Copy the following blocks into your empty model window:
 - An Inport block, from the Sources library, to initiate the input signal whose value the Simulink Design Verifier software controls
 - A Compare To Zero block to provide simple logic, from the Logic and Bit Operations library
 - An Outport block to receive the output signal, from the Sinks library
- 3** Connect these blocks such that your model appears similar to the following.



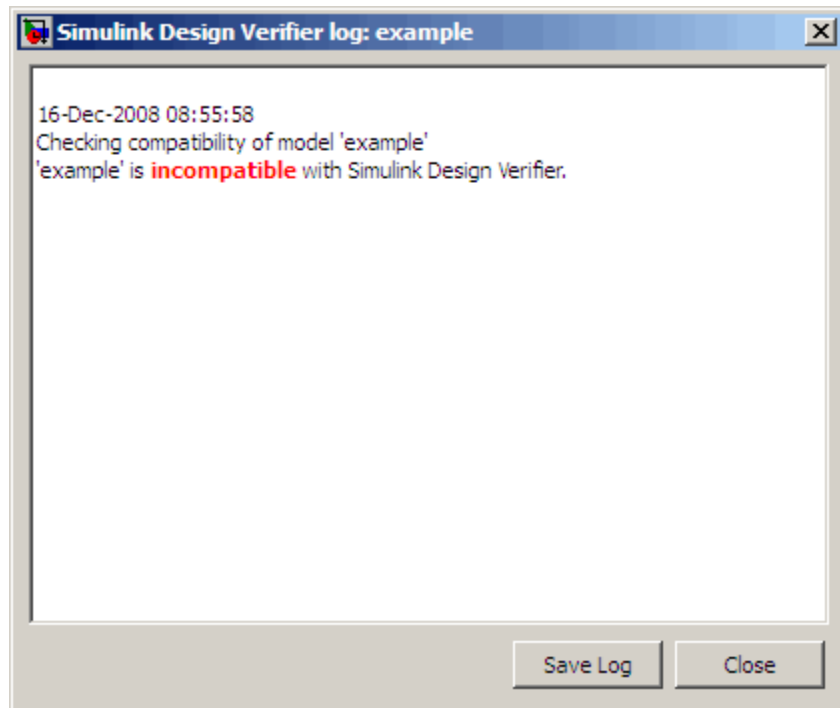
4 Save your model as `example.mdl` for use in the next task.

Checking Compatibility of the Example Model

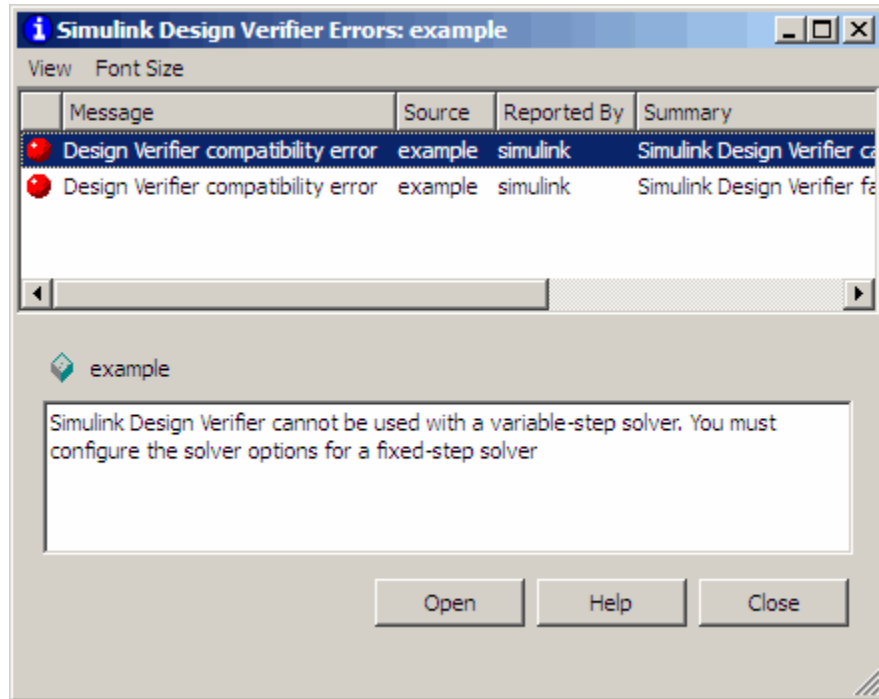
In this task, you ensure that a model is compatible for use with the Simulink Design Verifier software. Specifically, you check the compatibility of the simple Simulink model that you created in the previous task. To complete this task, perform the following steps:

1 In your Simulink model window, select **Tools > Design Verifier > Check Model Compatibility**.

The Simulink Design Verifier software displays the following log window, which indicates that your model is incompatible.



It also displays the following incompatibility error in the Simulation Diagnostics Viewer.

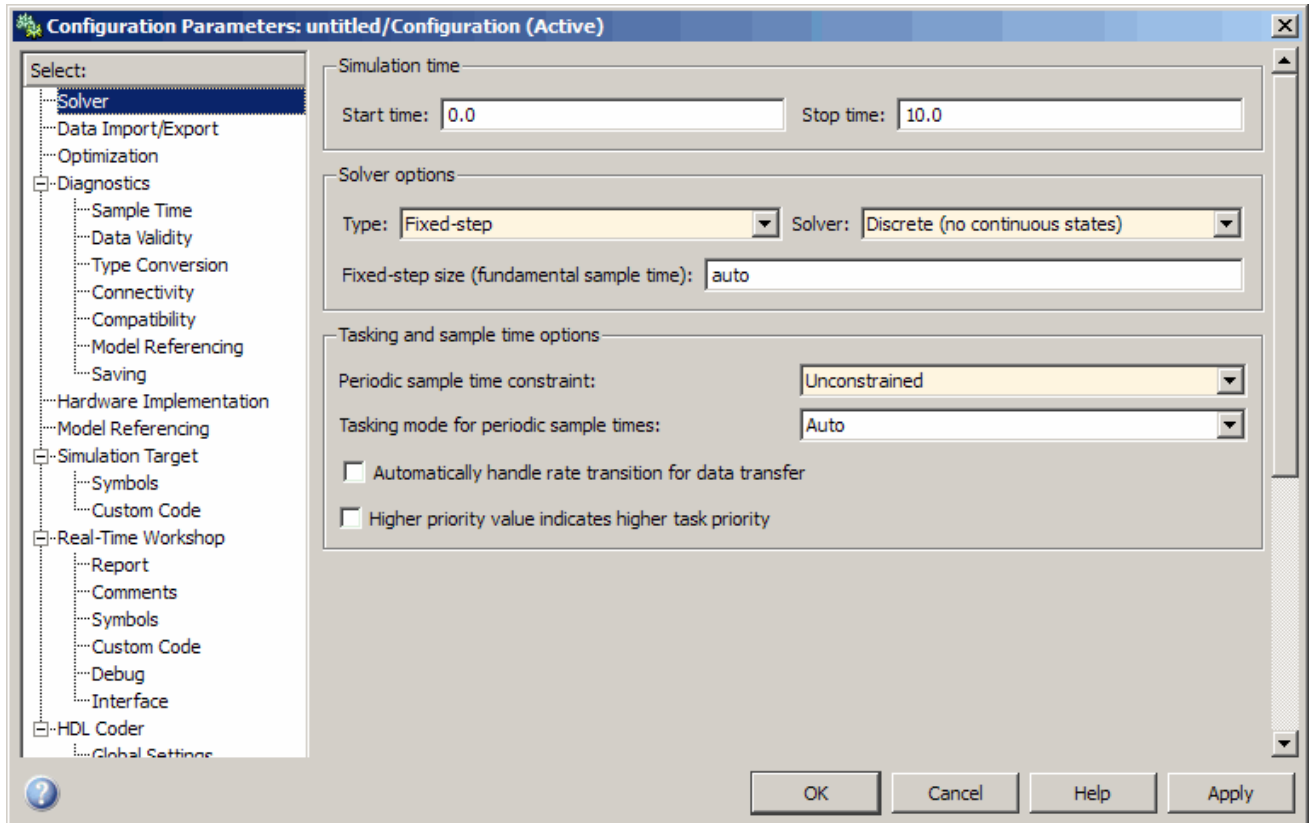


The error message informs you that the Simulink Design Verifier software does not support variable-step solvers. To work around this incompatibility, you must use a fixed-step solver.

- 2 In your Simulink model window, select **Simulation > Configuration Parameters**.

The Configuration Parameters dialog box appears.

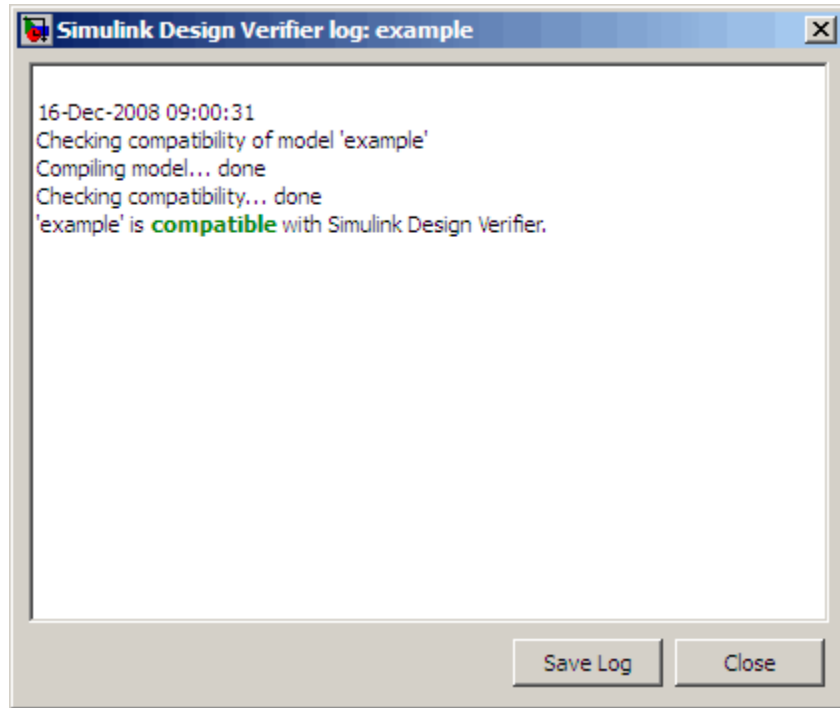
- 3 In the **Select** tree on the left side of the Configuration Parameters dialog box, click the **Solver** category (if not already selected). Under **Solver options** on the right side, set the **Type** option to **Fixed-step**, and then set the **Solver** option to **Discrete (no continuous states)**.



4 Click **Apply** and **OK** to apply your changes and close the Configuration Parameters dialog box.

5 Recheck the compatibility of your model. In your Simulink model window, select **Tools > Design Verifier > Check Model Compatibility**.

The Simulink Design Verifier software displays the following log window, which confirms that your model is compatible for analysis.



6 Save your `example.mdl` model for use in the next task.

What If a Model Is Partially Compatible?

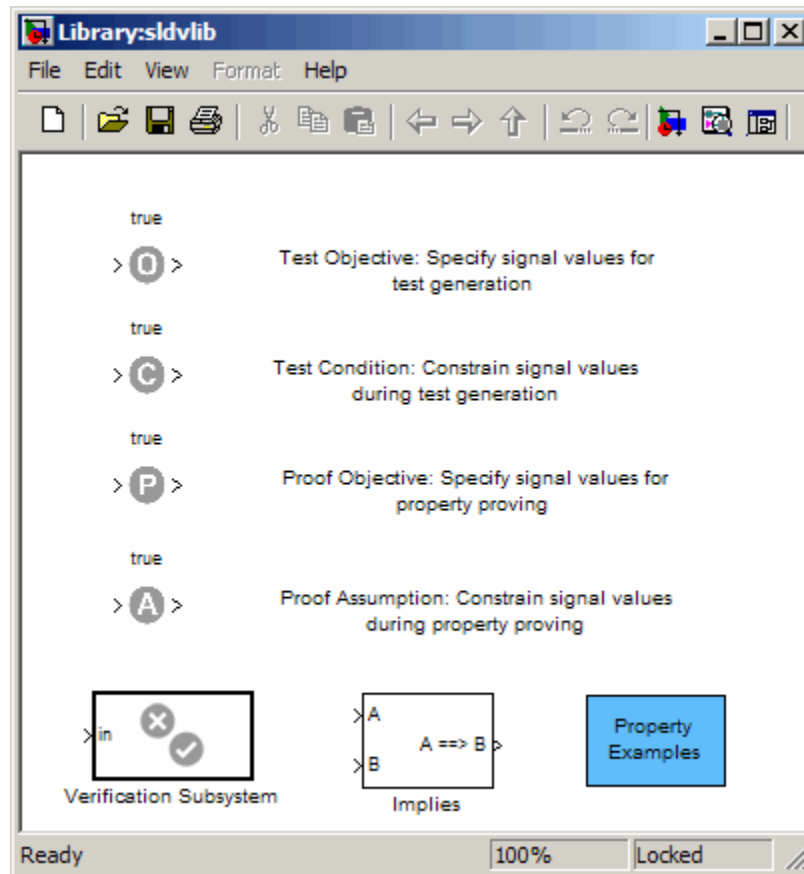
If the compatibility check indicates that your model is partially compatible, your model contains at least one element that is incompatible with the Simulink Design Verifier software. You can continue analyzing a partially compatible model if you turn on automatic stubbing. For details, see “Handling Incompatibilities with Automatic Stubbing” on page 2-6.

Instrumenting the Example Model

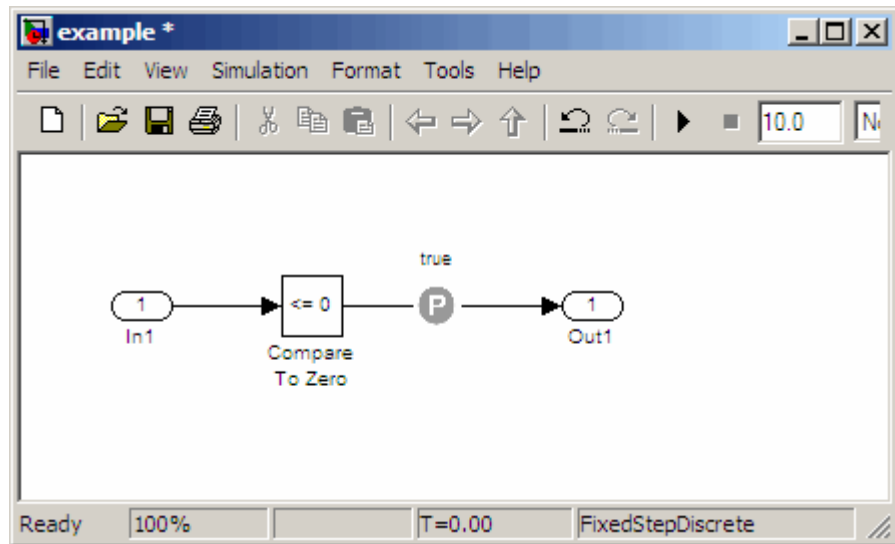
In this task, you prepare your example model so that you can prove its properties with the Simulink Design Verifier software. Specifically, you instrument the model by adding and configuring a Proof Objective block. To complete this task, perform the following steps:

- 1 In the MATLAB Command Window, enter `sldvlib`.

The Simulink Design Verifier library appears.



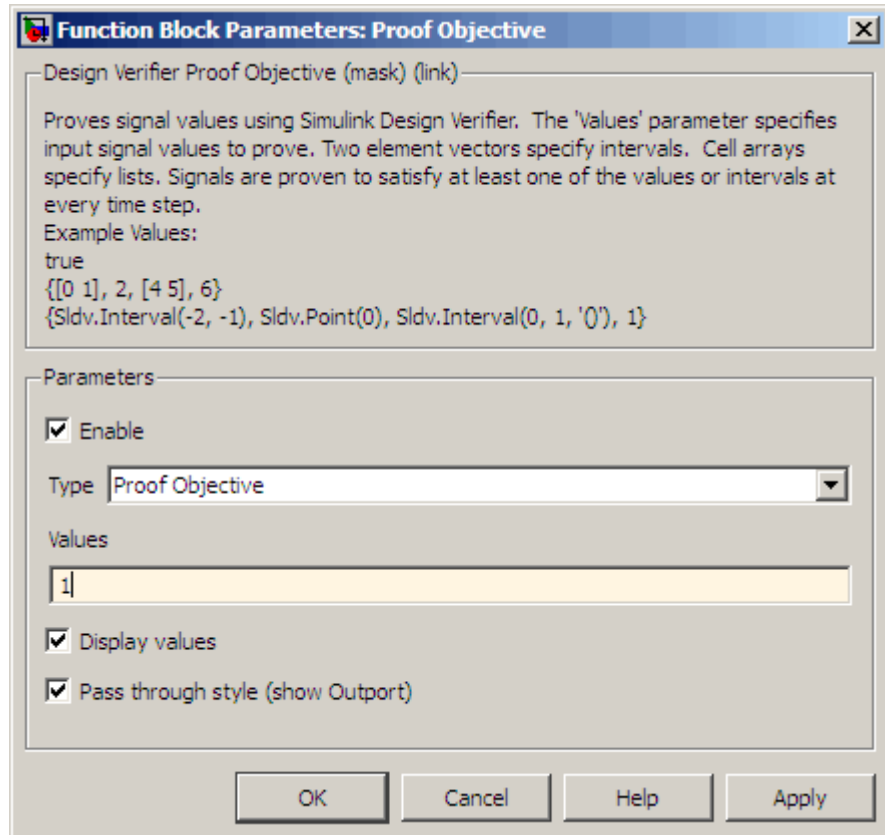
- 2 Copy the Proof Objective block to your model by dragging it from the Simulink Design Verifier library to your model window.
- 3 In your model window, insert the Proof Objective block between the Compare To Zero and Outport blocks (see "Inserting Blocks in a Line" in the Simulink documentation for help with this step).



- 4 Double-click the Proof Objective block in your model to access its attributes.

The Proof Objective block parameter dialog box appears.

- 5 In the **Values** box, enter 1. The Simulink Design Verifier software will attempt to prove that the signal output by the Compare To Zero block always attains this value for any signals that it receives.



6 Click **Apply** and **OK** to apply your changes and close the Proof Objective block parameter dialog box.

7 Save your `example.mdl` model for use in the next task.

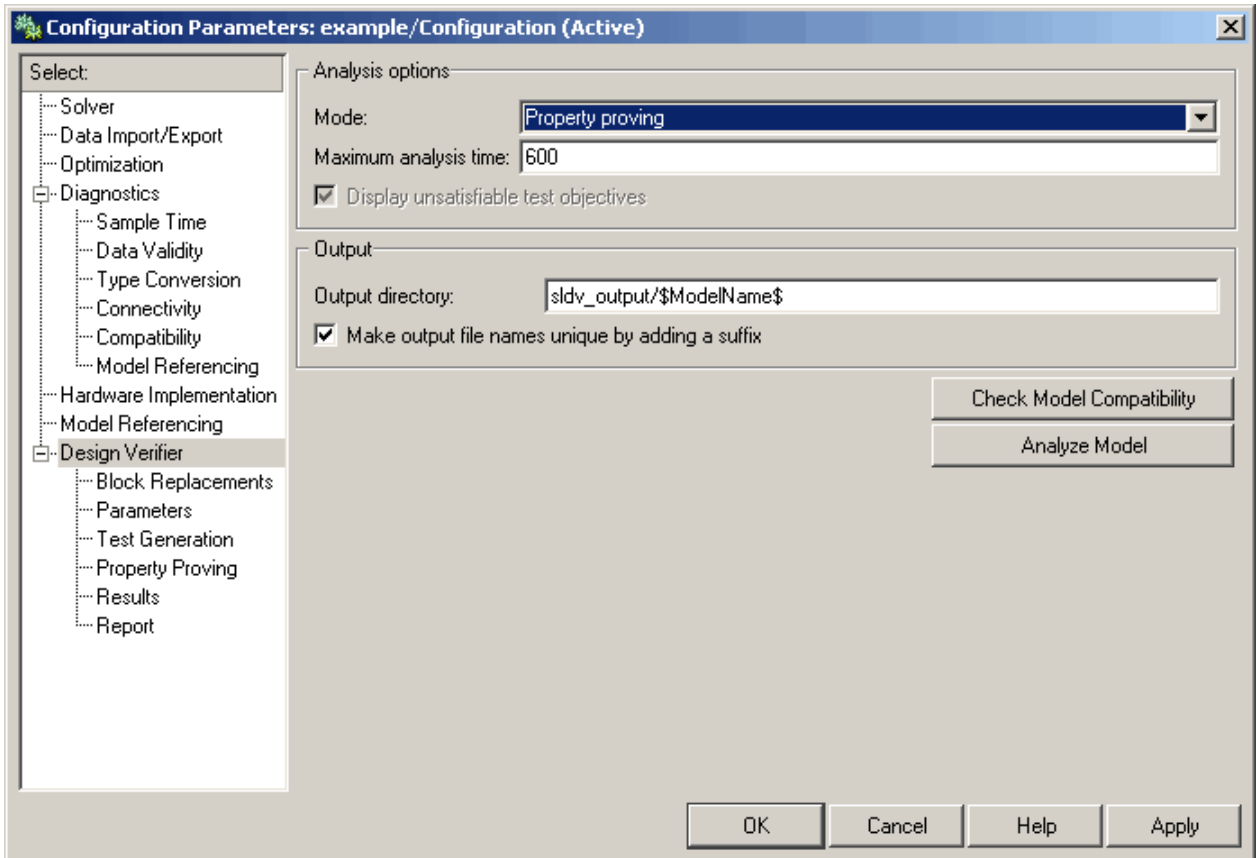
Configuring Property-Proving Options

In this task, you configure the Simulink Design Verifier software to prove properties of the simple Simulink model that you instrumented. To complete this task, perform the following steps:

1 In your Simulink model window, select **Tools > Design Verifier > Options**.

The Simulink Design Verifier software displays its options in the Configuration Parameters dialog box.

- 2 In the **Select** tree on the left side of the Configuration Parameters dialog box, select the **Design Verifier** category. Under **Analysis options** on the right side, set the **Mode** option to Property proving.



- 3 Click **Apply** and **OK** to apply your changes and close the Configuration Parameters dialog box.

Note Using the **Property Proving** pane, you can optionally specify values for other parameters that control how the Simulink Design Verifier software proves properties of your model. See “Property Proving Pane” on page 6-12 for more information.

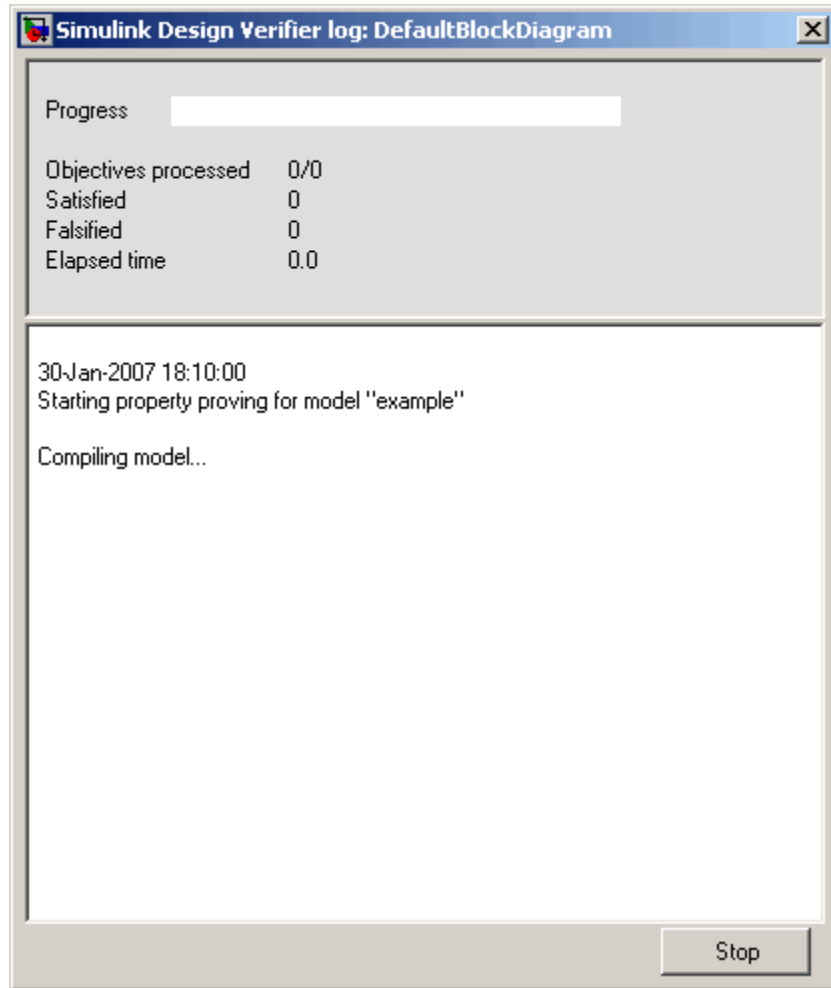
4 Save your `example.mdl` model for use in the next task.

Analyzing the Example Model

In this task, you execute the Simulink Design Verifier analysis. The software proves a property of your example model and produces results for you to interpret. To complete this task, perform the following steps:

1 In your Simulink model window, select **Tools > Design Verifier > Prove Properties**.

The Simulink Design Verifier software begins analyzing your model to prove its properties. During its analysis, the software displays a log window.



The Simulink Design Verifier log window updates you on the progress of the proof, providing information such as the number of objectives processed and how many of those objectives were either satisfied or falsified. Also, this dialog box includes a **Stop** button that you can click to terminate the proof at any time.

When the Simulink Design Verifier software completes its analysis, it displays the following items:

- Simulink Design Verifier report — an HTML report named `example_report.html`.
- Test harness — a harness model named `example_harness.mdl`.
- Signal Builder dialog box — Signals that falsify the proof objective in this model.

The remaining steps in this section help you interpret the results that you obtained.

- 2 Review the Simulink Design Verifier report. The report includes the following **Table of Contents** whose items you can click to navigate to particular chapters and sections.

Table of Contents	
1. Summary	
2. Analysis Information	
3. Proof Objectives Status	
4. Properties	

- 3 In the **Table of Contents**, click Summary.

Chapter 1. Summary	
Analysis Information	
Model:	example
Mode:	PropertyProving
Status:	Completed normally
Objectives Status	
Number of Objectives:	1
Objectives Falsified with Counterexamples:	1

The Summary provides an overview of the analysis results, and it indicates that the Simulink Design Verifier software identified a counterexample that falsifies an objective in your model.

- 4 Scroll back to the top of the browser window. In the **Table of Contents**, click **Proof Objectives Status**.

Objectives Falsified with Counterexamples				
#:	Type	Model Item	Description	Counterexample
1	Custom Proof Objective	Proof Objective	Objective: 1	1

The Objectives Falsified with Counterexamples table lists the proof objectives that the Simulink Design Verifier software disproved using a counterexample it generated. You can locate the objective in your model window by clicking **Proof Objective**; the software highlights the corresponding Proof Objective block in your model window.

- 5 In the Objectives Falsified with Counterexamples table under the **Counterexample** column, click 1.

Proof Objective

Summary

Model Item: [Proof Objective](#)

Property: Objective: 1

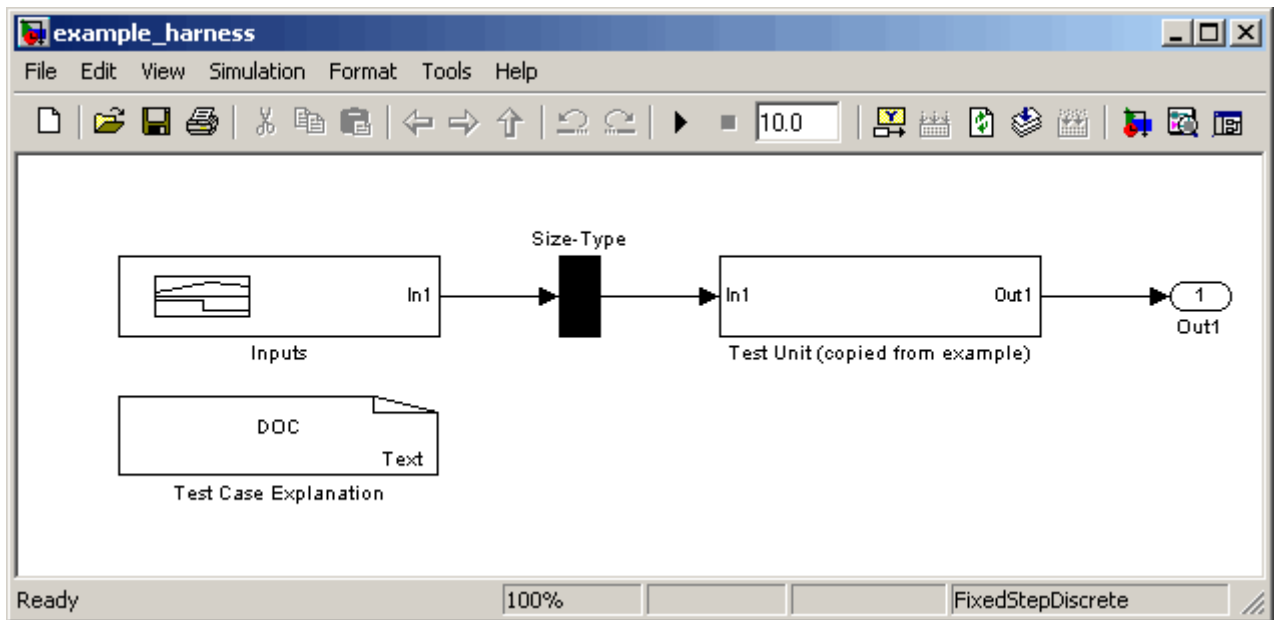
Status: Falsified

Counter Example

Time	0
Step	1
In1	99

This section displays information about proof objective 1 and provides details about the counterexample that the Simulink Design Verifier software generated to disprove that objective. In this counterexample, a signal value of 99 falsifies the objective that you specified using the Proof Objective block. That is, 99 is not less than or equal to 0, which causes the Compare To Zero block to return 0 (false) instead of 1 (true).

6 Review the harness model named `example_harness.mdl`.



The harness model contains the following items:

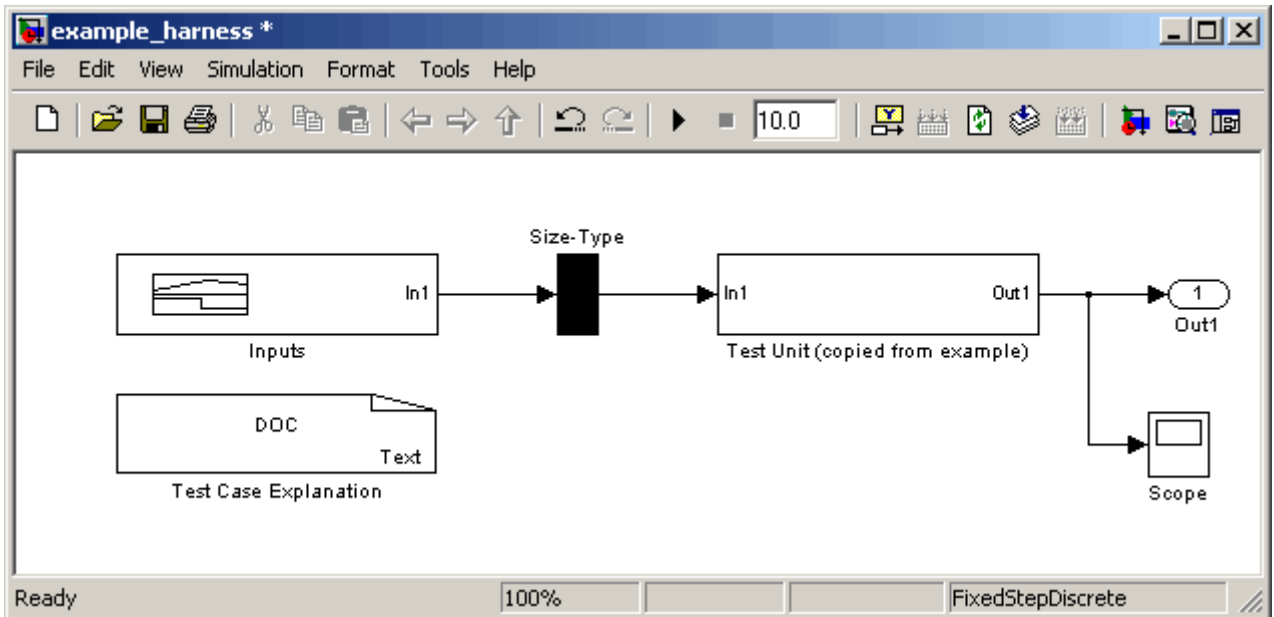
- Signal Builder block named **Inputs** — A group of signals that falsify proof objectives.
- Subsystem block named **Test Unit** — A copy of your model.
- DocBlock named **Test Case Explanation** — A textual description of the counterexamples that the software generates.

Note See the *Simulink Reference* for more information about interacting with blocks such as the Signal Builder, Subsystem, and DocBlock.

You can simulate the harness model to observe the counterexample that falsifies the proof objective in your model:

- 7 In the MATLAB Command Window, enter `simulink` to open the Simulink library.
- 8 From the Sinks library, copy a Scope block into your harness model window. The Scope block allows you to see the value of the signal output by the Compare To Zero block in your model.
- 9 In your harness model window, connect the output signal of the Test Unit subsystem to the Scope block.

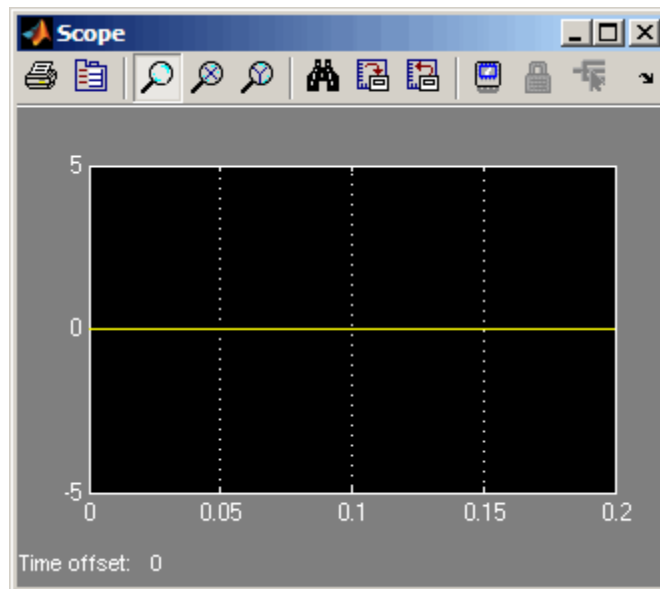
Your model should appear similar to the following:



- 10 In your harness model window, select **Simulation > Start** to begin the simulation.

The Simulink software simulates the harness model.

- 11 In your harness model window, double-click the Scope block to open its display window.



The Scope block displays the value of the signal output by the Compare To Zero block in your model. In this example, the Compare To Zero block returns 0 (false) throughout the simulation. Recall that you specified that the proof objective in your model is 1 (true). Hence, the counterexample that the Signal Builder block supplies falsifies the proof objective.

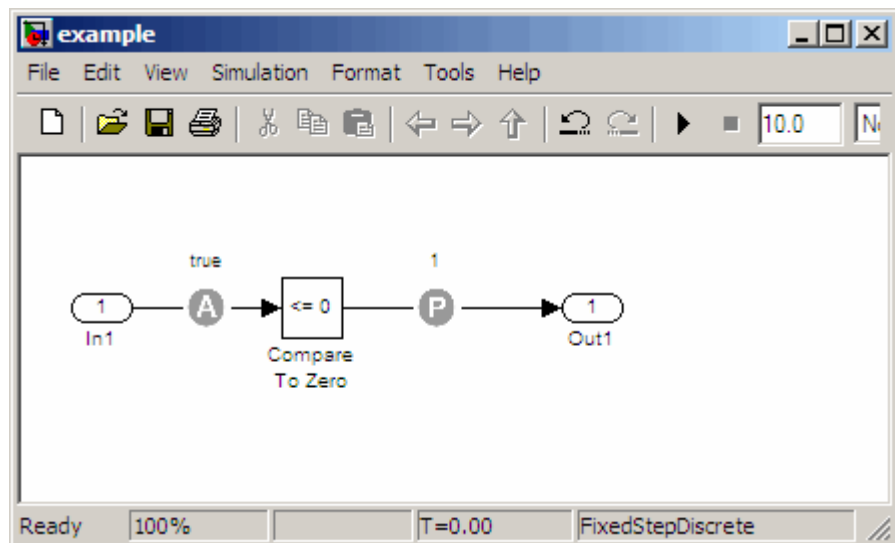
Customizing the Example Proof

In this task, you modify the simple Simulink model whose proof objective the Simulink Design Verifier software disproved in the previous task. Specifically, you customize the proof by adding and configuring a Proof Assumption block. To complete this task, perform the following steps:

- 1 If the Simulink Design Verifier library is not already open, type `sldvlib` in the MATLAB Command Window.

The Simulink Design Verifier library appears.

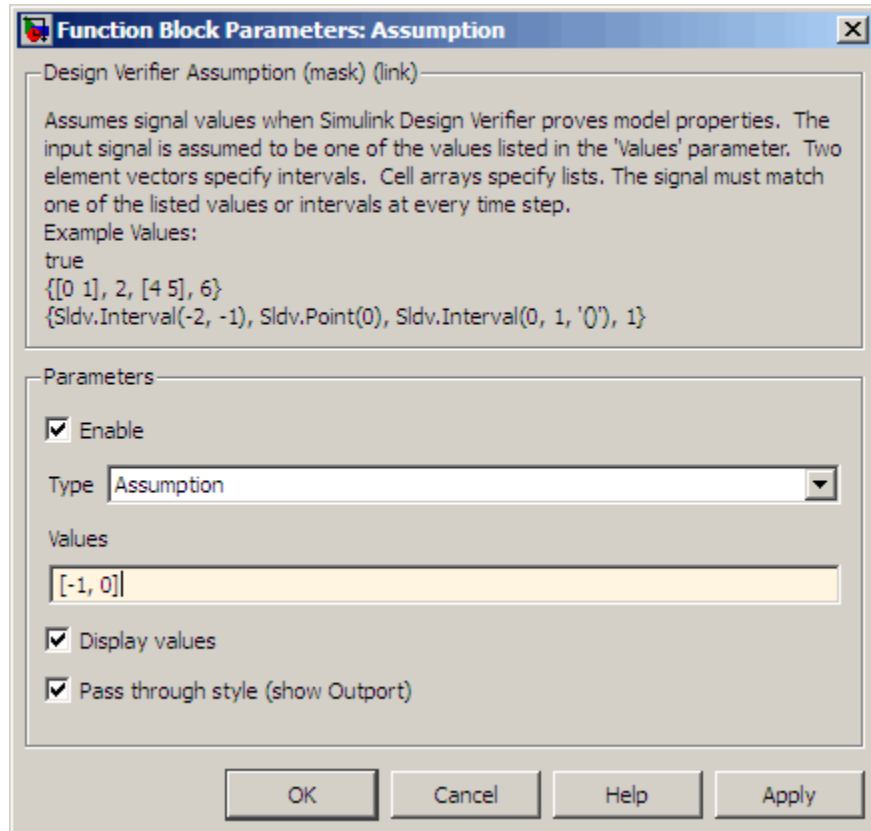
- 2 Copy the Proof Assumption block to your model (`example.mdl`) by dragging it from the Simulink Design Verifier library to your model window.
- 3 In your model window, insert the Proof Assumption block between the Inport and Compare To Zero blocks.



- 4 Double-click the Proof Assumption block in your model to access its attributes.

The Proof Assumption block parameter dialog box appears.

- 5 In the **Values** box, enter `[-1, 0]`. When proving properties of this model, the Simulink Design Verifier software will constrain the signal values entering the Compare To Zero block to the specified interval.



6 Click **Apply** and **OK** to apply your changes and close the Proof Assumption block parameter dialog box.

7 Save your `example.mdl` model for use in the next task.

Simulink Design Verifier blocks are preserved with a model, even if you open the model on a MATLAB installation that does not have a Simulink Design Verifier license. If you then open the model on a system with a Simulink Design Verifier license, the software can analyze the model with the blocks and options that you originally added to the model.

Reanalyzing the Example Model

In this task, you execute the Simulink Design Verifier analysis on the model that you modified. To observe how Proof Assumption blocks affect proofs, compare the result of this analysis to the result that you obtained in a previous task. To complete this task, perform the following steps:

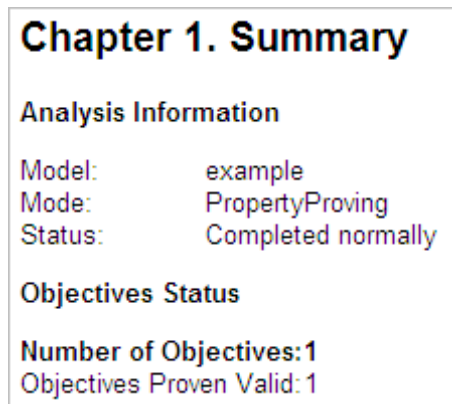
- 1 In your Simulink model window, select **Tools > Design Verifier > Prove Properties**.

The Simulink Design Verifier software displays a log window and begins analyzing your model to prove its properties.

When the software completes the analysis, it displays a new Simulink Design Verifier report named `example_report1.html`.

Note If the Simulink Design Verifier software satisfies all proof objectives in your model, it does not generate a harness model.

- 2 Review the Simulink Design Verifier report.
- 3 In the **Table of Contents**, click Summary.



Chapter 1. Summary

Analysis Information

Model: example
Mode: PropertyProving
Status: Completed normally

Objectives Status

Number of Objectives: 1
Objectives Proven Valid: 1

The Summary chapter of indicates that the Simulink Design Verifier software proved an objective in your model.

- 4 Scroll back to the top of the browser window. In the **Table of Contents**, click **Proof Objectives Status**.

Objectives Proven Valid				
#:	Type	Model Item	Description	Counterexample
1	Custom Proof Objective	Proof Objective	Objective: 1	n/a

The Objectives Proven Valid table lists the proof objectives that the Simulink Design Verifier software proved to be valid.

- 5 Scroll down to view the Properties chapter or go to the top of the browser window and click **Properties** in the **Table of Contents**.

Proof Objective	
Summary	
Model Item:	Proof Objective
Property:	Objective: 1
Status:	Proven valid

The Proof Objective summary indicates that the Simulink Design Verifier software proved an objective that you specified in your model. Because the Proof Assumption block restricted the domain of the input signals to the interval $[-1, 0]$, the software was able to prove that this interval contains no values that are greater than zero, thereby satisfying the proof objective.

Analyzing Contradictory Models

If the analysis produces the error **The model is contradictory in its current configuration**, the software detected a contradiction in your model and it cannot analyze the model. You can have a contradiction if your model has Proof Assumption blocks with incorrect parameters, for example, an assumption that states that a signal has to be between 0 and 5 when the signal is constant 10.

If the software detects a contradiction, all previous results are invalidated and the software reports that all the properties are falsified.

Proving Properties in a Subsystem

If you have a large model, you can prove the properties of a subsystem in the model and review the analyses in smaller, manageable reports. The workflow for proving properties in a subsystem is as follows:

- 1** Open the model that contains the subsystem.
- 2** Make the subsystem atomic.
- 3** Run the Simulink Design Verifier software using the **Prove Properties of Subsystem** option.
- 4** Review the results.

The tutorial in “Analyzing a Subsystem” on page 1-26 explains how to generate test cases for the Controller subsystem in the Cruise Control Test Generation model. The steps for proving properties are similar, except that you select the **Prove Properties of Subsystem** option instead of the **Generate Tests for Subsystem** option.

Proving Complex Properties

Property-Proving Examples

The Simulink Design Verifier block library includes four Simulink examples that allow you to prove complex properties:

- “Conditions that Trigger a Result” on page 8-30
- “Conditions That Cannot Be True Simultaneously” on page 8-31
- “Increasing or Decreasing Signals” on page 8-31
- “Conditions with One True Element” on page 8-32

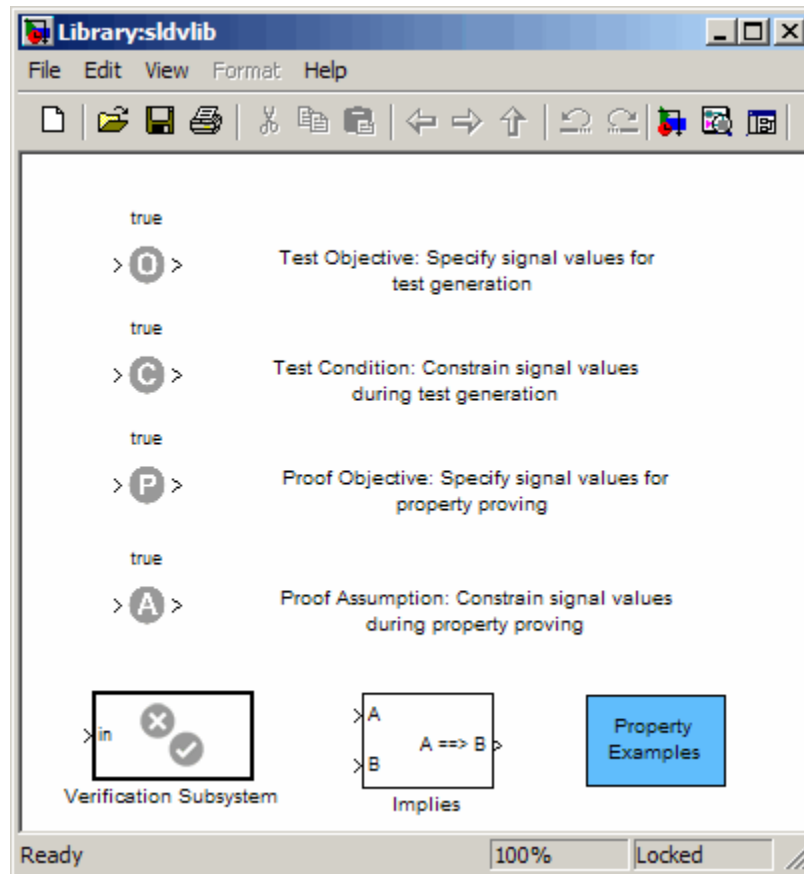
The workflow for using these examples in your model is:

- 1** Copy these examples into your verification subsystem.
- 2** Adapt them, if necessary, for the specific properties you are trying to prove.
- 3** Run the Simulink Design Verifier analysis to prove the assertions in these examples never fail.
- 4** If the assertion fails, the software looks for a counterexample that causes the assertion to fail and generates a harness model.
- 5** Execute the counterexample on the harness model to confirm that the assertion fails with that counterexample.

To view these examples:

- 1** Open the block library. Type:

```
sldvlib
```



2 Double-click **Property Examples** to open the examples.

Simulink Design Verifier Property Examples

The screenshot displays five examples of property assertions in Simulink Design Verifier:

- Implies:** A block labeled 'A ==> B' receives two inputs: 'condition' (value 1) and 'result' (value 2). The output is an 'Assertion' block with a checkmark.
- Increasing:** A signal 'increasing' (value 7) passes through a 'delay' block (1/z) and then a 'gte' (greater than or equal to) block to an 'Assertion2' block.
- Decreasing:** A signal 'decreasing' (value 8) passes through a 'delay' block (1/z) and then a 'lte' (less than or equal to) block to an 'Assertion3' block.
- Exclusivity:** Four modes (mode5, mode6, mode7, mode8) with values 9, 10, 11, and 12 enter a 'Logic Value1' block (~= 0). The output goes to a 'Sum1' block (Σ), then a 'check1' block (<= 1), and finally an 'Assertion4' block.
- Mutual Exclusivity:** Four modes (mode1, mode2, mode3, mode4) with values 3, 4, 5, and 6 enter a 'Logic Value' block (~= 0). The output goes to a 'Sum' block (Σ), then a 'check' block (== 1), and finally an 'Assertion1' block.

Implies operation describes conditions that should trigger a result.

Increasing and decreasing operations describe signals that should increase or decrease.

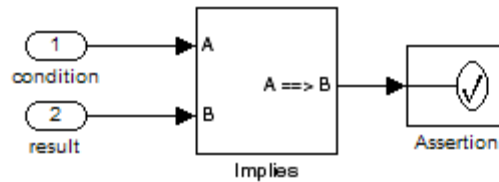
Exclusivity operation describes conditions that should never be true at same time.

Mutual exclusivity operation describes conditions that should have exactly one true element.

Ready 100% FixedStepDiscrete

Conditions that Trigger a Result

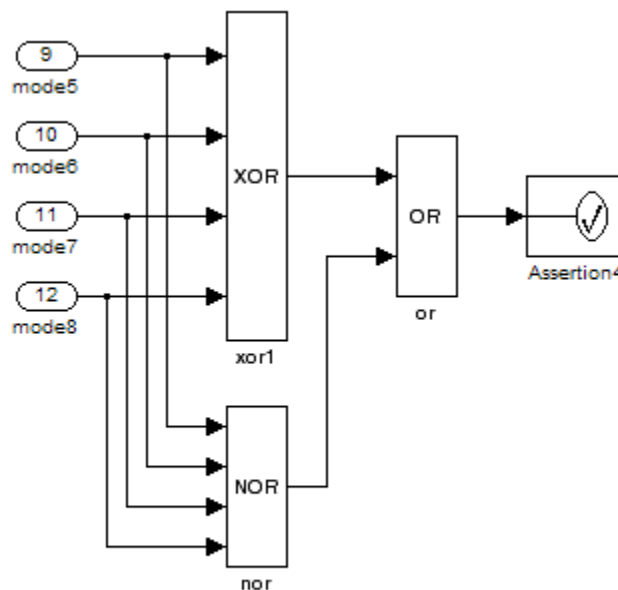
The Simulink Design Verifier Implies block allows you to test for conditions that trigger a result. This example specifies that if condition A is true, result B must always be true.



Implies operation describes conditions that should trigger a result.

Conditions That Cannot Be True Simultaneously

This example specifies that the four inputs must never all be true at the same time.

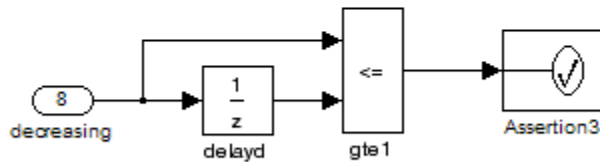
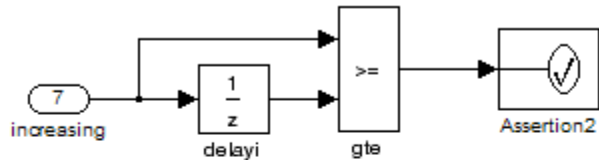


Exclusivity operation describes conditions that should never be true at same time.

Increasing or Decreasing Signals

The two examples in this section specify that a signal is either:

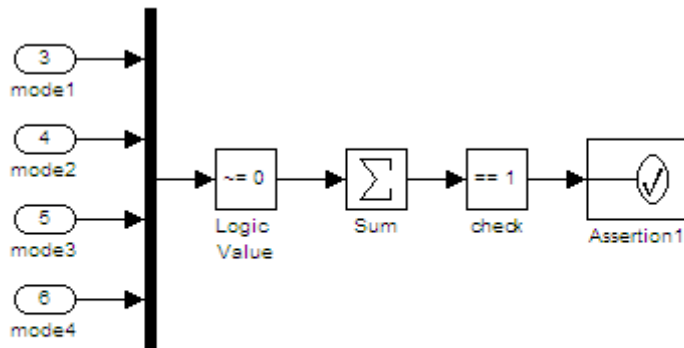
- Always increasing or staying constant
- Always decreasing or staying constant



Increasing and decreasing operations describe signals that should increase or decrease.

Conditions with One True Element

This example specifies that only one of the four input signals can be true.



Mutual exclusivity operation describes conditions that should have exactly one true element.

Reviewing the Results

The Simulink Design Verifier software produces several artifacts after it analyzes your model. Depending on the analysis, the software can generate a data file, a test harness model, a SystemTest file, and a report. The following sections describe each of these items:

- “Examining Simulink® Design Verifier Data Files” on page 9-2
- “Exploring Test Harness Models” on page 9-8
- “Creating a SystemTest TEST-File” on page 9-15
- “Understanding Simulink® Design Verifier Reports” on page 9-18

Examining Simulink Design Verifier Data Files

In this section...

“About Simulink® Design Verifier Data Files” on page 9-2

“Overview of the sldvData Structure” on page 9-2

“Model Information Fields in sldvData” on page 9-3

“Simulating Models with Simulink® Design Verifier Data Files” on page 9-7

About Simulink Design Verifier Data Files

When you enable the **Save test data to file** parameter (see “Results Pane” on page 6-14), the Simulink Design Verifier software generates a data file when it completes its analysis. The data file is a MAT-file that contains a structure named `sldvData`. This structure stores all the data the software gathers and produces during the analysis. Although the software displays the same data graphically in the test harness model and report, you can use the data file to conduct your own analysis or to generate a custom report.

Overview of the sldvData Structure

When the Simulink Design Verifier software completes its analysis, it produces a MAT-file that contains a structure named `sldvData`. To explore the contents of the `sldvData` structure:

- 1 Generate test cases for the `sldvdemo_flipflop` model (see “Analyzing a Model” on page 1-6).
- 2 To load the data file, at the MATLAB prompt, enter the following command:

```
load('sldv_output\sldvdemo_flipflop\sldvdemo_flipflop_sldvdata.mat')
```

The MATLAB software loads the `sldvData` structure into its workspace. This structure contains the Simulink Design Verifier analysis results of the `sldvdemo_flipflop` model.

- 3 Enter `sldvData` to display the field names that constitute the structure:

```
sldvData =
```

```

ModelInformation: [1x1 struct]
AnalysisInformation: [1x1 struct]
  ModelObjects: [1x2 struct]
    Objectives: [1x12 struct]
      TestCases: [1x4 struct]
        Version: '1.4'

```

See “Structures” in the MATLAB documentation for more information about working with structures.

Model Information Fields in sldvData

The following sections describe the fields in the sldvData structure:

- “ModelInformation Field” on page 9-3
- “AnalysisInformation Field” on page 9-4
- “ModelObjects Field” on page 9-4
- “Objectives Field” on page 9-5
- “TestCases Field / CounterExamples Field” on page 9-5
- “Version Field” on page 9-7

ModelInformation Field

In the sldvData structure, the ModelInformation field contains information about the model you analyzed. The following table describes each subfield of the ModelInformation field.

Subfield Name	Description
Name	String specifying the model name.
Version	String specifying the model number.
Author	String specifying the user name.
SubsystemPath	String representing the full path name of the subsystem (if any) that was analyzed.
ReplacementModel	String specifying the name of the model (if any) that contains the block replacements.

AnalysisInformation Field

In the `sldvData` structure, the `AnalysisInformation` field lists settings of particular analysis options and related information. The following table describes each subfield of the `AnalysisInformation` field.

Subfield Name	Description
Status	String specifying the completion status of the Simulink Design Verifier analysis.
Options	Deep copy of the Simulink Design Verifier options object used during the analysis.
InputPortInfo	Cell array of structures specifying information about each Inport block in the top-level system.
OutputPortInfo	Cell array of structures specifying information about each Outport block in the top-level system.
SampleTimes	For internal use only.

ModelObjects Field

In the `sldvData` structure, the `ModelObjects` field lists the model items and their associated objectives. The following table describes each subfield of the `ModelObjects` field.

Subfield Name	Description
descr	String specifying the full path to a model object, including objects in a Stateflow chart.
typeDesc	String specifies the block type of the model object.
s1Path	String specifying the full path to a Simulink model object.
sfObjType	String specifying the type of a Stateflow object, e.g., S for state and T for transition.
sfObjNum	Integer representing the unique identifier of a Stateflow object.
objectives	Vector of integers representing the indices of objectives associated with a model object.

Objectives Field

In the `sldvData` structure, the `Objectives` field lists information about each objective, such as its type, status, and description. The following table describes each subfield of the `Objectives` field.

Subfield Name	Description
<code>type</code>	String specifying the type of an objective.
<code>status</code>	String specifying the status of an objective.
<code>descr</code>	String specifying the description of an objective.
<code>label</code>	String specifying the label of an objective.
<code>outcomeValue</code>	Integer specifying an objective's outcome.
<code>coveragePointIdx</code>	Integer representing the index of a coverage point with which an objective is associated.
<code>modelObjectIdx</code>	Integer representing the index of a model object with which an objective is associated.
<code>testCaseIdx</code>	Integer representing the index of a test case or counterexample that addresses an objective.

TestCases Field / CounterExamples Field

In the `sldvData` structure, this field can have two names, depending on the type of check:

- If you set the **Mode** parameter to `Test generation`, the `TestCases` field lists information about each test case, such as its signal values and the test objectives it achieves.
- If you set the **Mode** parameter to `Property proving`, the `CounterExamples` field lists information about each counterexample and the proof objective it falsifies.

The following table describes each subfield of the `TestCases / CounterExamples` field.

Subfield Name	Description
timeValues	Vector specifying the time values associated with signals in a test case or counterexample.
dataValues	Cell array specifying the data values associated with signals in a test case or counterexample.
paramValues	<p>Structure specifying the parameter values associated with a test case or counterexample. Its fields include:</p> <p>name — String specifying the name of a parameter.</p> <p>value — Number specifying the value of a parameter.</p> <p>noEffect — Logical value specifying whether a parameter's value affects an objective.</p>
stepValues	Vector specifying the number of time steps that comprise signals in a test case or counterexample.
objectives	<p>Structure specifying objectives that a test case or a counterexample addresses. Its fields include:</p> <p>objectiveIdx — Integer representing the index of an objective that a test case achieves or a counterexample falsifies.</p> <p>atTime — Time value at which either a test case achieves an objective or a counterexample falsifies an objective.</p> <p>atStep — Time step at which either a test case achieves an objective or a counterexample falsifies an objective.</p>

Subfield Name	Description
dataNoEffect	Cell array of logical vectors specifying whether a signal's data values affect an objective. The vector uses 1 to indicate that a signal's data value does not affect an objective; otherwise, it uses 0.
expectedOutput	Cell array of vectors specifying the output values that result from simulating the model using the test case signals. Each cell represents the output values associated with a different Output block in the top-level system. This subfield is populated if you select Include expected output values .

Version Field

In the `sldvData` structure, the `Version` field is a string specifying the version of the Simulink Design Verifier software that verified the model.

Simulating Models with Simulink Design Verifier Data Files

The `sldvruntest` function simulates a model using test cases or counterexamples that reside in a Simulink Design Verifier data file. For example, suppose the following command specifies the location of the data file that the Simulink Design Verifier software produced after analyzing the `sldvdemo_flipflop` model (see “Analyzing a Model” on page 1-6):

```
sldvDataFile = 'sldv_output\sldvdemo_flipflop\sldvdemo_flipflop_sldvdata.mat'
```

Use the `sldvruntest` function to simulate the `sldvdemo_flipflop` model using test case 2 in the data file:

```
output = sldvruntest('sldvdemo_flipflop', sldvDataFile, 2)
```

For more information, see the `sldvruntest` reference page.

Exploring Test Harness Models

In this section...
“About Test Harness Models” on page 9-8
“Anatomy of a Test Harness” on page 9-8
“Configuration of the Test Harness” on page 9-13
“Simulating the Test Harness” on page 9-13

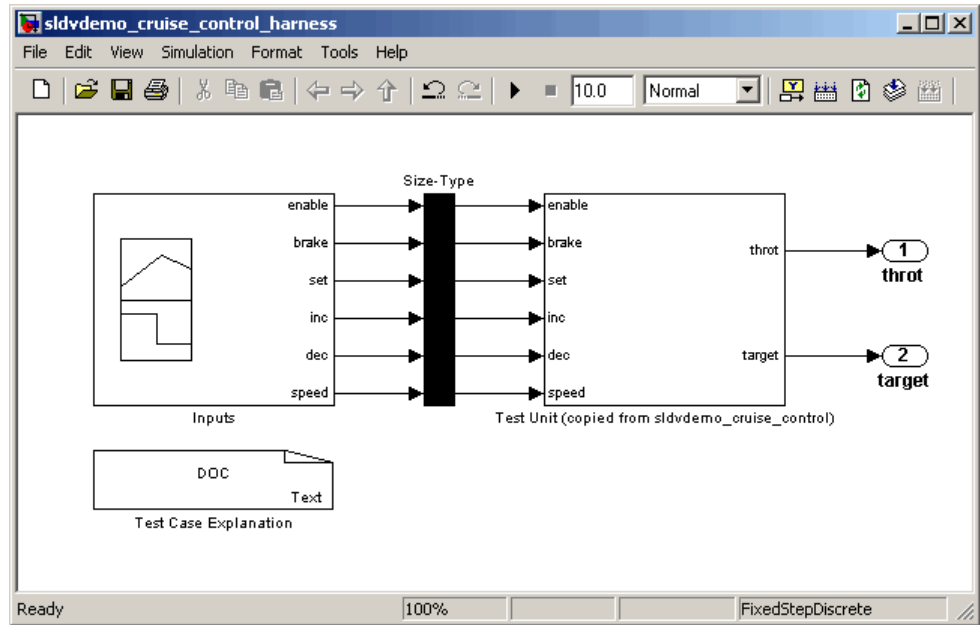
About Test Harness Models

When you enable the **Save test harness as model** parameter (see “Results Pane” on page 6-14), the Simulink Design Verifier software generates a test harness model after it completes its analysis. If the software’s **Mode** parameter specifies **Test generation**, the harness model contains test cases that achieve test objectives. Otherwise, the software’s **Mode** parameter specifies **Property proving** and the harness model contains counterexamples that falsify proof objectives.

Note The Simulink Design Verifier software can generate a harness model only when the top level of the system you are analyzing contains an Inport block.

Anatomy of a Test Harness

When the Simulink Design Verifier software completes its analysis, it produces a test harness model that looks like this:



The harness model contains the following items:

- Test Case Explanation** — This DocBlock block documents the test cases or counterexamples that the Simulink Design Verifier software generates. Double-click the Test Case Explanation block to view a description of each test case or counterexample. The block lists either the test objectives that each test case achieves (as in the next graphic) or the proof objectives that each counterexample falsifies.

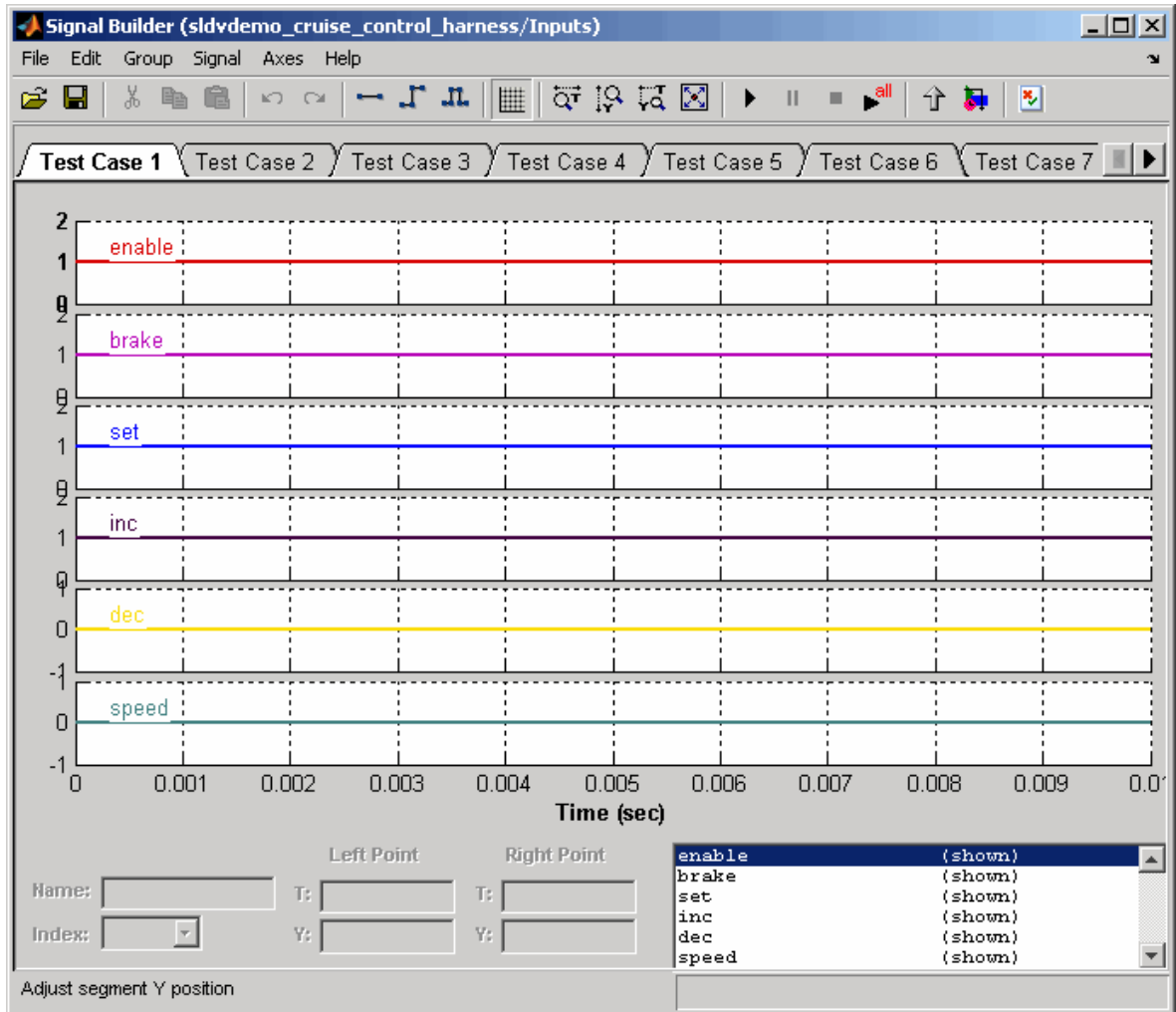
```

Editor - C:\TEMP\docblock-2513-00012207.txt
File Edit Text Go Tools Debug Desktop Window Help
+ - 1.0 + ÷ 1.1 x % %
1 |Test Case 1 (8 Objectives)
2 |   Parameter values:
3 |
4 |   1. Controller/PI Controller - enable logical value F @ T=0.00
5 |   2. Controller/Switch1 - logical trigger input true (output is from 1s
6 |   3. Controller/Logical Operator1 - Logic: input port 1 T @ T=0.00
7 |   4. Controller/Logical Operator2 - Logic: input port 1 T @ T=0.00
8 |   5. Controller/Logical Operator2 - Logic: MCDC expression for output w
9 |   6. Controller/Logical Operator - Logic: input port 1 T @ T=0.00
10 |  7. Controller/Logical Operator - Logic: input port 2 F @ T=0.00
11 |  8. Controller/Logical Operator - Logic: MCDC expression for output wi
12 |
13 |Test Case 2 (3 Objectives)
14 |   Parameter values:
15 |
16 |   1. Controller/Logical Operator1 - Logic: input port 1 F @ T=0.00
17 |   2. Controller/Logical Operator - Logic: input port 1 F @ T=0.00
18 |   3. Controller/Logical Operator - Logic: MCDC expression for output wi
19 |
20 |Test Case 3 (6 Objectives)
21 |   Parameter values:
22 |
plain text file Ln 1 Col 1 OVR

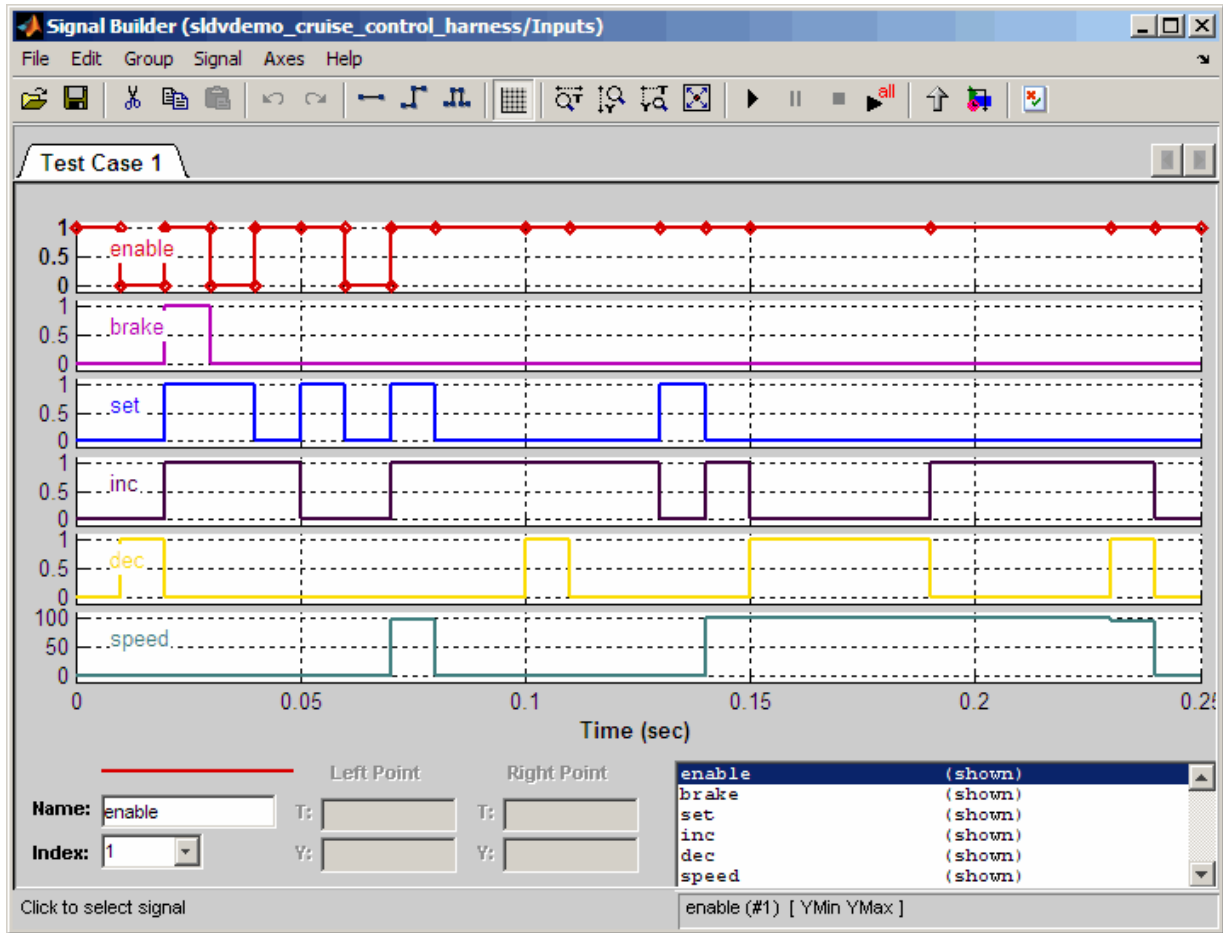
```

- **Inputs** — This Signal Builder block contains signals that comprise the test cases or counterexamples that the Simulink Design Verifier software generated. Double-click the Inputs block to open the Signal Builder dialog box and view its signals. The following Signal Builder block shows the signals for Test Case 8 after analyzing the `sldvdemo_cruise_control` model with the default options.

Each signal group represents a unique test case or counterexample. In the Signal Builder dialog box, select a tab to view the signals associated with a particular test case or counterexample.



If you select the Long test cases option of the **Test suite optimization** parameter, the analysis creates fewer, longer test cases. For example, if you select the Long test cases option for the `sldvdemo_cruise_control` model, the analysis produces 1 long test case instead of 10 shorter test cases. The following Signal Builder dialog box shows the signals for that test case.



Note For more information about the Signal Builder dialog box, see “Working with Signal Groups” in *Simulink User’s Guide*.

- **Size-Type** — This Subsystem block transmits signals from the Inputs block to the Test Unit block. It ensures that the signals are of the appropriate size and data type, which the Test Unit block expects.

- **Test Unit** — This Subsystem block contains a copy of the original model that the Simulink Design Verifier software analyzed.

Configuration of the Test Harness

After the Simulink Design Verifier software generates the test harness, it has the following settings:

- The test harness start time is always 0. If the original model uses a nonzero start time, the software ignores this and always uses 0 for the simulation start time for test cases and counterexamples.
- The test harness stop time always equals the stop time of the longest test case in the Signal Builder dialog box.
- By default, the software enables coverage reporting for test harness models that contain test cases. Although it enables coverage reporting with particular options selected, you can customize the settings to meet your needs. For more information, see “Model Coverage Reporting Options” in the *Simulink Verification and Validation User’s Guide*.

Simulating the Test Harness

The test harness model enables you to simulate a copy of your original model using the test cases or counterexamples that the Simulink Design Verifier software generates. Using the test harness model, you can simulate:

- A counterexample
- A single test case, for which the Simulink Verification and Validation software collects and displays model coverage information
- All test cases, for which the Simulink Verification and Validation software collects and displays cumulative model coverage information


To simulate a single test case or counterexample:

- 1** In the test harness model, double-click the Inputs block.

The Signal Builder dialog box appears.

- 2** In the Signal Builder dialog box, select the tab associated with a particular test case or counterexample.

The Signal Builder dialog displays the signals that comprise the selected test case or counterexample.


- 3** In the Signal Builder dialog box, click the **Start simulation** button 

The Simulink software simulates the test harness model using the signals associated with the selected test case or counterexample. When simulating a test case, the Simulink Verification and Validation software collects model coverage information and displays a coverage report.

To simulate all test cases and measure their combined model coverage:

- 1** In the test harness model, double-click the Inputs block.

The Signal Builder dialog box appears.

- 2** In the Signal Builder dialog box, click the **Run all** button 

The Simulink software simulates the test harness model using all test cases, while the Simulink Verification and Validation software collects model coverage information and displays a coverage report.

When you click **Run all**, the software simulates all the test cases using the stop time for the test harness model. The stop time equals the stop time for the longest test case, so you may accumulate additional coverage when you simulate the shorter test cases.

See “Simulating with Signal Groups” in *Simulink User’s Guide* for more information about simulating models containing Signal Builder blocks.

Creating a SystemTest TEST-File

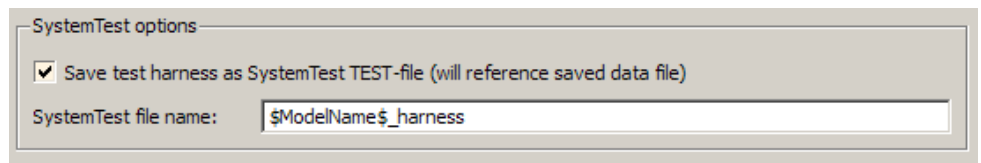
If you have installed the SystemTest software with your MATLAB application, you can specify that the Simulink Design Verifier software create a SystemTest TEST-file when it analyzes a model. Creating a TEST-file allows you to configure and collect model coverage results and run the test cases from inside the SystemTest environment.

Note The option to create a SystemTest TEST-file is only available in test-generation mode; you cannot create this file when running a property-proving analysis.

In addition, if you have a model with a large number of inputs, this feature eliminates the overhead of creating the test harness. However, you can create both a test harness and a TEST-file in the same analysis.

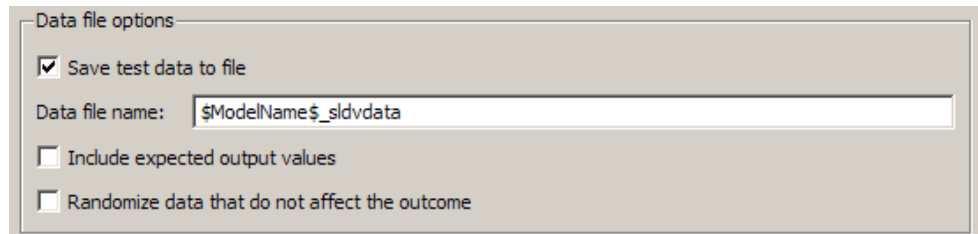
To create a TEST-file for the `sldvdemo_cruise_control` model, perform these steps:

- 1 Type `sldvdemo_cruise_control` at the MATLAB command prompt to open the Cruise Control Test Generation model.
- 2 Select **Simulation > Configuration Parameters** to open the Configuration Parameters dialog box.
- 3 In the **Select** pane, under **Design Verifier**, select **Results**.
- 4 On the **Results** pane, under **SystemTest options**, select **Save test harness as SystemTest TEST-file (will reference saved data file)**.

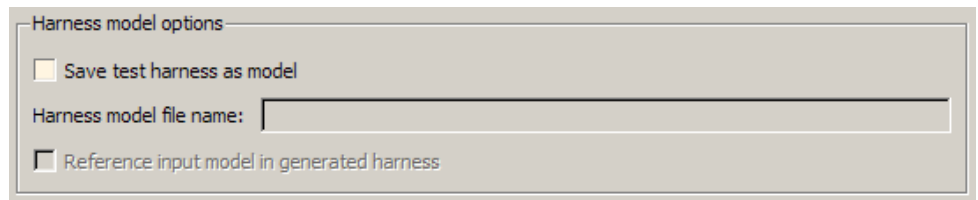


- 5 If you prefer a file name other than the default, specify the **SystemTest file name**.

- 6 Under **Data File options**, verify that **Save test data to file** is selected. You must select this option to generate a TEST-file.

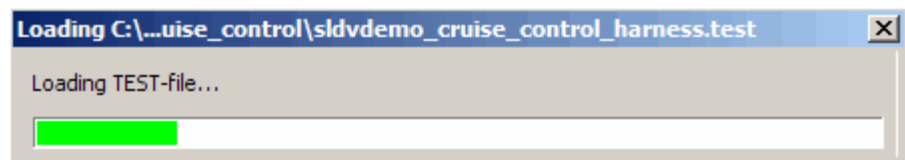


- 7 If you do not need the Simulink Design Verifier test harness in addition to the TEST-file, under **Harness model options**, clear **Save test harness as model**.



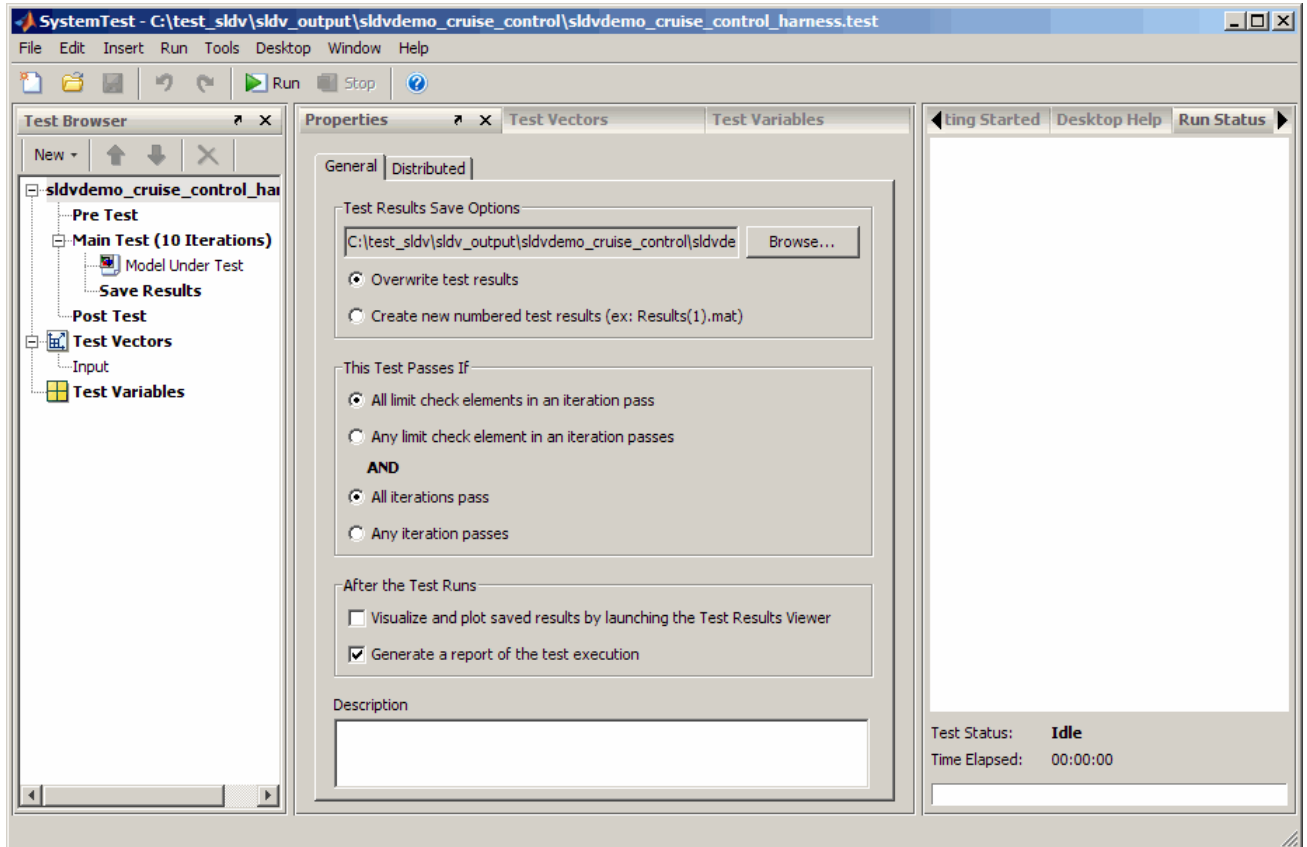
- 8 Click **Apply** and **OK** to save the changes and exit the Configuration Parameters dialog box.
- 9 Double-click the Run block in the `sldvdemo_cruise_control` model to start the analysis.

When the software is creating the TEST-file, the following status box appears.



When the analysis completes, the SystemTest desktop opens the TEST-file, which, for this example, is saved as

```
matlabroot\sldvdemo_output\sldv_cruise_control\sldvdemo_cruise_control_harness.test
```



In the **Test Browser** pane, the 10 iterations under Main Test correspond to the 10 test cases the Simulink Design Verifier software generates and describes in the Test Case Explanation block of the test harness.

For information about running the test cases using the SystemTest software, see “Creating a Simulink Design Verifier Data File Test Vector” in the *SystemTest User’s Guide*.

Understanding Simulink Design Verifier Reports

In this section...

“About Simulink® Design Verifier Reports” on page 9-18

“Front Matter” on page 9-18

“Summary Chapter” on page 9-19

“Analysis Information Chapter” on page 9-20

“Test / Proof Objectives Status Chapter” on page 9-25

“Model Items Chapter” on page 9-29

“Test Cases / Properties Chapter” on page 9-29

About Simulink Design Verifier Reports

When you enable the **Generate report of the results** parameter (see “Report Pane” on page 6-17), the Simulink Design Verifier software generates an HTML report after it completes its analysis. If the software’s **Mode** parameter specifies **Test generation**, the report describes the model’s test objectives and any corresponding test cases that result from the analysis. Otherwise, the software’s **Mode** parameter specifies **Property proving**, and the report describes the model’s proof objectives and any counterexamples that result from the analysis.

Front Matter

The report begins with two sections: title and table of contents.

Simulink Design Verifier Report

sldvdemo_cruise_control

slemaire

17-Dec-2008 09:59:43

Table of Contents

- [1. Summary](#)
- [2. Analysis Information](#)
- [3. Test Objectives Status](#)
- [4. Model Items](#)
- [5. Test Cases](#)

The title section lists the following information:

- Model or subsystem name the Simulink Design Verifier software analyzed
- User name associated with the current MATLAB session
- Date and time that the Simulink Design Verifier software generated the report

The table of contents follows the title section. Clicking items in the table of contents allows you to navigate quickly to particular chapters and sections.

Summary Chapter

The Summary chapter of the HTML report provides an overview of the Simulink Design Verifier analysis.

Chapter 1. Summary

Analysis Information

Model: sldvdemo_cruise_control
Mode: TestGeneration
Status: Completed normally

Objectives Status

Number of Objectives: 34
Objectives Satisfied: 34

Analysis Information Chapter

The Analysis Information chapter of the HTML report includes the following sections:

- “Model Information” on page 9-20
- “Analysis Options” on page 9-21
- “Unsupported Blocks” on page 9-22
- “Constraints” on page 9-22
- “Block Replacements Summary” on page 9-23
- “Approximations” on page 9-24

Model Information

The Model Information section provides the following information about the current version of the model:

- Path and file name of the model that the Simulink Design Verifier software analyzed
- Model version
- Date and time that the model was last saved
- Name of the person who last saved the model

Model Information

File:	C:\test_sldv\sldvdemo_flipflop.mdl
Version:	1.15
Time Stamp:	Fri Jun 27 15:38:15 2008
Author:	slemaire

See “Managing Model Versions” in *Simulink User’s Guide* for details about specifying this information for your models.

Analysis Options

The Analysis Options section provides information about the Simulink Design Verifier analysis settings.

The Analysis Options section lists the parameters that affected the Simulink Design Verifier analysis. See “sldvoptions Object Parameters” on page 11-11 for more information about the parameters that this section displays.

Analysis Options

Mode:	TestGeneration
Test Suite Optimization:	CombinedObjectives
Maximum Testcase Steps:	500 time steps
Test Conditions:	UseLocalSettings
Test Objectives:	UseLocalSettings
Model Coverage Objectives:	MCDC
Maximum Processing Time:	60s
Block Replacement:	on
Block Replacement Rules:	<FactoryDefaultRules>
Parameters Analysis:	on
Parameters Configuration File:	sldv_params_template.m
Save Data:	on
Save Harness:	on
Save Report:	on

Unsupported Blocks

If your model includes unsupported elements, you can turn on automatic stubbing to allow the analysis to proceed. If you turn on automatic stubbing, the software considers only the interface of the unsupported elements, not their actual behavior. This technique allows the software to complete the analysis. However, the analysis may achieve only partial results if any of the unsupported model elements affect the simulation outcome.

The Unsupported Blocks section appears only if the analysis stubbed any unsupported elements; it lists the unsupported elements in a table, with a link to the element in the model.

Unsupported Blocks

The following blocks are not supported by Simulink Design Verifier. They were abstracted during the analysis. This can lead Simulink Design Verifier to produce only partial results for parts of the model that depends on the output values of these blocks.

Block	Type
Trigonometric Function	Trigonometry

For more information about automatic stubbing, see “Handling Incompatibilities with Automatic Stubbing” on page 2-6.

Constraints

The Constraints section provides information about any test conditions that the Simulink Design Verifier software applied when it analyzed a model.

You can locate the constraint in your model by clicking constraint; the software highlights the corresponding Test Condition block in your model window and opens a new window showing the block in detail.

Constraints	
Name	Constraint
constraint	[0, 100]

Block Replacements Summary

The Block Replacements Summary provides an overview of the block replacements that the Simulink Design Verifier software executed. It appears only if the Simulink Design Verifier software replaced any blocks in a model.

Each row of the table corresponds to a particular block replacement rule that the Simulink Design Verifier software applied to the model. The table lists the following:

- Name of the M-file that represents the block replacement rule and the value of the `BlockType` parameter the rule specifies
- Description of the rule that the `MaskDescription` parameter of the replacement block specifies
- Names of any blocks that the Simulink Design Verifier software replaced in the model

To locate a particular block replacement in your model, click on the name for that replacement in the Replaced Blocks column of the table; the software highlights the affected block in your model window and opens a new window that displays the block in detail.

Block Replacements Summary

Table 2.1. Block Replacements

#:	Replacement Rule / Block Type	Rule Description	Replaced Blocks
1	blkrep_rule_lookup_normal.m /Lookup	Inserts test objectives for each interval of 1-D lookup table blocks.	Lookup Table
2	blkrep_rule_switch_normal.m /Switch	Inserts test objectives for switch blocks that require each switch position be demonstrated when the values of input ports 1 and 3 differ.	Switch
3	sldvdemo_custom_blkrep_rule_sqrt.m /Math	Approximates the mathematical function sqrt using lookup table. The input range is constrained to [0 10000].	Math Function

See Chapter 4, “Working with Block Replacements” for more information.

Approximations

Each row of the Approximations table describes a specific type of approximation that the Simulink Design Verifier software used during its analysis of the model.

Approximations

Simulink Design Verifier performed the following approximations during analysis. These can impact the precision of the results generated by Simulink Design Verifier. Please see the product documentation for further details.

	Type	Description
1	Rational approximation	The model includes floating-point arithmetic. Simulink Design Verifier approximates floating-point arithmetic with rational number arithmetic.

Note Review the analysis results carefully when the software uses approximations. In rare cases, an approximation may result in test cases that fail to achieve test objectives or counterexamples that fail to falsify proof objectives. For example, a floating-point-roundoff error might prevent a signal from exceeding a designated threshold value.

Test / Proof Objectives Status Chapter

The Test / Proof Objectives Status chapter of the HTML report summarizes all test or proof objectives in a model, including an objective's type, the model item to which it corresponds, and its description. This chapter displays each objective in one of the following tables associated with the objective's status:

- **Objectives Undecided** — Lists the test or proof objectives for which the Simulink Design Verifier software was unable to determine an outcome in the allotted time. In this property-proving example, either the software exceeded its analysis time limit (which the **Maximum analysis time** parameter specifies), or you aborted the analysis before it completed processing these objectives.

Objectives Undecided

Simulink Design Verifier was not able to process these objectives with the current options.

#:	Type	Model Item	Description	Counterexample
1	Custom Proof Objective	Verify Output/FoutCorrect	Objective: T	n/a
2	Custom Proof Objective	Verify Output/ToutCorrect	Objective: T	n/a

- **Objectives Producing Errors** — Lists the test or proof objectives for which the Simulink Design Verifier software encountered errors during its analysis. In this example, analyzing these objectives involves nonlinear arithmetic, which the software does not support. Thus, errors occur and appear in the report.

Objectives Producing Errors

#:	Type	Model Item	Description	Test Case
4	Decision	Mode switch	logical trigger input true (output is from 1st input port)	n/a
8	Decision	Basic Roll Mode/Integrator	integration result <= lower limit T	n/a
10	Decision	Basic Roll Mode/Integrator	integration result >= upper limit T	n/a

If the Simulink Design Verifier software’s **Mode** parameter specifies Test generation, the Status section also includes the following tables:

- **Objectives Proven Unsatisfiable** — Lists the test objectives that the Simulink Design Verifier software determined could not be satisfied. In this example, the software found that there are no test cases that achieve these objectives.

Objectives Proven Unsatisfiable

Simulink Design Verifier proved that there does not exist any test case exercising these test objectives. This often indicates the presence of dead-code in the model. Other possible reasons can be inactive blocks in the model due to parameter configuration or test constraints such as given using Test Condition blocks. In rare cases, the approximations performed by Simulink Design Verifier can make objectives impossible to achieve.

#:	Type	Model Item	Description	Test Case
1	Custom Test Objective	True	Objective: 100	n/a

- **Objectives Satisfied** — Lists test objectives that the Simulink Design Verifier software satisfied. In this example, the software generated test cases that achieve the specified objectives.

Objectives Satisfied

Simulink Design Verifier found test cases that exercise these test objectives.

#:	Type	Model Item	Description	Test Case
1	Decision	PI Controller	enable logical value F	2
2	Decision	PI Controller	enable logical value T	1
3	Decision	P Controller	enable logical value F	1
4	Decision	P Controller	enable logical value T	2
5	Decision	mp switch	integer input value = 1 (output is from input port 2)	1
6	Decision	mp switch	integer input value = 2 (output is from input port 3)	2

- **Objectives Satisfied - No Test Case** — Lists test objectives that the Simulink Design Verifier software satisfied without generating test cases.

Objectives Satisfied - No Test Case

#:	Type	Model Item	Description	Test Case
2	Decision	Saturation	input > lower limit T	n/a
3	Decision	Saturation	input >= upper limit F	n/a
4	Decision	Saturation	input >= upper limit T	n/a

If the Simulink Design Verifier software's **Mode** parameter specifies Property proving, the Status section includes:

- **Objectives Proven Valid** — Lists the proof objectives that the Simulink Design Verifier software proved valid.

Objectives Proven Valid

#:	Type	Model Item	Description	Counterexample
1	Custom Proof Objective	Proof Objective	Objective: 1	n/a

- **Objectives Falsified with Counterexamples** — Lists the proof objectives that the Simulink Design Verifier software disproved. In this example, the software generated at least one counterexample that falsifies the specified objectives.

Objectives Falsified with Counterexamples

#:	Type	Model Item	Description	Counterexample
1	Assert	Verify True Output/Assertion	assert	1

- **Objectives Falsified - No Counterexample** — Lists the proof objectives that the Simulink Design Verifier software disproved without generating counterexamples. This occurs if, for example, you specified a proof objective on a signal whose value the software cannot control, or the software encountered a divide-by-zero error when instantiating a counterexample.

Objectives Falsified - No Counterexample

#:	Type	Model Item	Description	Counterexample
1	Custom Proof Objective	Proof Objective	Objective: F	n/a
2	Custom Proof Objective	Proof Objective1	Objective: T	n/a

Model Items Chapter

The Model Items chapter of the HTML report includes a table for each object in the model that defines coverage objectives. The table for a particular object lists all of the associated objectives, the objective types, objective descriptions, and the status of each objective at the end of the analysis.

The table for an individual object in the model will look similar to this one for the TK switch in the Roll Reference subsystem.

To highlight a given object in your model, click [View](#) at the upper-left corner of the table; the software opens a new window that displays the object in detail. To view the details of the test case that was applied to a specific objective, click the test case number in the last column of the table.

Roll Reference/TK switch

[View](#)

#:	Type	Description	Status	Test Case
27	Decision	logical trigger input false (output is from 3rd input port)	Produced error	n/a
28	Decision	logical trigger input true (output is from 1st input port)	Satisfied	1

Test Cases / Properties Chapter

The Test Cases / Counterexamples chapter of the HTML report provides an overview of the test cases or counterexamples that the Simulink Design

Verifier software generated during its analysis. Depending on whether the software's **Mode** parameter specifies **Test generation** or **Property proving**, this chapter includes sections associated with the following:

- “Test Cases” on page 9-30
- “Properties” on page 9-35

Test Cases

If the Simulink Design Verifier software's **Mode** parameter specifies **Test generation**, the report's Test Cases chapter includes sections that summarize the test cases the analysis generated, one per test case.

Chapter 4. Test Cases

Table of Contents

[Test Case 1](#)

[Test Case 2](#)

This section contains detailed information about each generated test case.

Test Case 1

Summary

Length: 0.06 Seconds (7 sample periods)

Objective Count: 1

Objectives

Step	Time	Model Item	Objectives
7	0.06	True	Objective: 2

Generated Input Data

Time	0	0.01	0.02	0.03-0.05	0.06
Step	1	2	3	4-6	7
raw	128	1	128	1	128

Each section lists the following information about a test case:

- Length of the signals that comprise the test case
- Total number of test objectives that the test case achieves
- Time step and corresponding time at which the test case achieves particular test objectives, indicated as a range if the signal value does not change over those time steps
- Values of the signals that comprise the test case

Note The Generated Input Data table can display a dash (–) instead of a number as a signal value. In this case, the value of the signal at that time step does not affect the test objective. In the test harness model, the Inputs block represents these values with zeros unless you enable the **Randomize data that does not affect outcome** parameter (see “Randomize data that does not affect outcome” on page 6-15).

If you set the **Test suite optimization** option to **Combined objectives** (the default), the Test Cases chapter in the report may include individual information about many test cases.

Chapter 5. Test Cases

Table of Contents

[Test Case 1](#)

[Test Case 2](#)

[Test Case 3](#)

[Test Case 4](#)

This section contains detailed information about each generated test case.

Test Case 1

Summary

Length: 0 Seconds (1 sample periods)

Objective Count: 3

Objectives

Step	Time	Model Item	Objectives
1	0	D Flip-Flop/D Flip-Flop D Flip-Flop/D Flip-Flop D Flip-Flop/D Flip-Flop	SubSystem: enable T SubSystem: trigger edge occurred F SubSystem: MCDC trigger edge occurred while enabled with trigger edge occurred F

Generated Input Data

Time	0
Step	1
D	0
CLK	0
! CLR	1

If you set the **Test suite optimization** option to Long test cases, the Test Cases chapter in the report includes fewer sections about the longer test cases.

Chapter 5. Test Cases

Table of Contents

[Test Case 1](#)

This section contains detailed information about each generated test case.

Test Case 1

Summary

Length: 0.5 Seconds (6 sample periods)

Objective Count: 12

Objectives

Step	Time	Model Item	Objectives
1	0	D Flip-Flop/D Flip-Flop D Flip-Flop/D Flip-Flop	SubSystem: enable F trigger edge occurred while enabled F
2	0.1	D Flip-Flop/D Flip-Flop D Flip-Flop/D Flip-Flop/Logic D Flip-Flop/D Flip-Flop D Flip-Flop/D Flip-Flop D Flip-Flop/D Flip-Flop D Flip-Flop/D Flip-Flop	SubSystem: trigger edge occurred T Logic: input port 1 F SubSystem: MCDC trigger edge occurred while enabled with enable T SubSystem: MCDC trigger edge occurred while enabled with trigger edge occurred T SubSystem: enable T trigger edge occurred while enabled T
3	0.2	D Flip-Flop/D Flip-Flop D Flip-Flop/D Flip-Flop	SubSystem: trigger edge occurred F SubSystem: MCDC trigger edge occurred while enabled with trigger edge occurred F
4	0.3	D Flip-Flop/D Flip-Flop	SubSystem: MCDC trigger edge occurred while enabled with enable F
6	0.5	D Flip-Flop/D Flip-Flop/Logic	Logic: input port 1 T

Generated Input Data

Time	0	0.1	0.2	0.3	0.4	0.5
Step	1	2	3	4	5	6
D	0	0	0	0	1	-
CLK	0	1	0	1	0	1
! CLR	0	1	1	0	0	1

Properties

If the Simulink Design Verifier software's **Mode** parameter specifies Property proving, the report's Properties chapter includes a series of sections that summarize the proof objectives and any counterexamples the software generated.

If the software proves an objective is valid, this report chapter displays a summary section similar to this one.

Proof Objective

Summary

Model Item: [Proof Objective](#)

Property: Objective: 1

Status: Proven valid

If the software falsifies an objective, this report chapter has a summary section similar to the one in the following figure.

To highlight the proof objective in your model, click the Model Item name in the Summary section.

Verify True Output/Assertion

Summary

Model Item: [Verify True Output/Assertion](#)

Property: assert

Status: Falsified

Counter Example

Time0	
Step 1	
raw	128

Analyzing Large Models and Improving Performance

- “Sources of Model Complexity” on page 10-2
- “Analyzing a Large Model” on page 10-3
- “Generating Reports for Large Models” on page 10-8
- “Managing Model Data to Simplify the Analysis” on page 10-9
- “Partitioning Model Inputs and Generating Tests Incrementally” on page 10-13
- “Analyzing the Model Using a Bottom-Up Approach” on page 10-15
- “Analyzing Logical Operations” on page 10-16
- “Handling Models with Large State Spaces” on page 10-17
- “Handling Problems with Counters and Timers” on page 10-18
- “Techniques for Proving Properties of Large Models” on page 10-20

Sources of Model Complexity

Some model characteristics can cause problems with a Simulink Design Verifier analysis in the following ways:

- Complexity of model inputs due to:
 - Large number of inputs (The number of inputs can vary, depending on the individual model.)
 - Types of inputs (floating-point values, for example)
 - The way the inputs affect the model state and the objectives of the analysis
- Number of possible simulation paths through a model
- Portions of the model that cannot be reached
- Large signal count in the model

The following sections describe techniques designed to reduce the impact of this complexity and achieve the best performance from the Simulink Design Verifier software.

Most of these techniques focus on test generation for large models, but you can use many of them to prove the properties of a large model and generate counterexamples when a property is disproved. In addition, “Techniques for Proving Properties of Large Models” on page 10-20 describes specific techniques for proving properties in a large model.

Analyzing a Large Model

In this section...
“Types of Large Model Problems” on page 10-3
“Using the Default Parameter Values” on page 10-4
“Modifying the Analysis Parameters” on page 10-5
“Using the Large Model Optimization” on page 10-6
“Stopping the Analysis Before Completion” on page 10-6

Types of Large Model Problems

The Simulink Design Verifier software may encounter some of these problems when analyzing a large model:

- Unsatisfiable objectives — The software proved there are no test cases that exercise these test objectives, and thus did not generate any test cases.
- Undecided objectives — The software was not able to satisfy or falsify these objectives.
- Objectives with errors — The most common error occurs when a model component uses nonlinear arithmetic, which can affect a test objective.
- Cannot complete the analysis in the time allotted — This problem may indicate an area of your model where the software encountered problems, or you may need to increase value of the **Maximum analysis time** parameter.
- Analysis hangs — If the number of objectives processed remains constant for a considerable length of time, the software has likely encountered complexity between the model and its objectives.
- Does not achieve a high percentage of model coverage — When you ran the test cases on the test harness, the percentage of model coverage was insufficient for your design.

The next few sections describe the initial steps to take when analyzing a large model. Although these steps address test generation, you can use a similar approach when proving properties in a model.

Using the Default Parameter Values

When you generate test cases for a model, whether large or small, the first step is to analyze the model using the Simulink Design Verifier default parameter values:

- 1 Check to see if your model is compatible with the Simulink Design Verifier software, as described in Chapter 3, “Ensuring Compatibility with the Simulink® Design Verifier Software”.
- 2 Using the default parameter values, analyze the model. The following table lists three of the default parameter values.

Parameter	Default Value	Description
Maximum analysis time	600 (seconds)	If the analysis does not finish within the specified time, the analysis times out and terminates.
Test suite optimization	Combined objectives	Generates test cases that address more than one test objective (if possible).
Model coverage objectives	MCDC	Generates test cases that achieve modified condition/decision coverage (MCDC), which includes decision coverage (DC) and condition coverage (CC).nc

- 3 Review the following information in the Simulink Design Verifier log window while the analysis runs:
 - Number of objectives processed — How many objectives were processed? Did the analysis hang after processing a certain number of objectives? The answers to these questions might give you a clue about where a problem might lie.
 - Number of objectives satisfied/Number of objectives falsified — Which objectives were falsified?

- Time elapsed — Did the analysis time out, or did it finish within the specified maximum analysis time?
- 4 When the analysis completes, review the Simulink Design Verifier report. This report contains links to the model elements for satisfied and falsified objectives so you can see what portions of the model might have problems.
 - 5 If all the test objectives have been satisfied, run the test cases on the test harness to determine model coverage.

If model coverage is sufficient, you do not need to do anything else. If the coverage is not sufficient, take additional steps to improve the analysis performance, as described in the following sections.

Note A large percentage of falsified objectives and poor model coverage often indicates that you need to change model parameter values to get complete coverage. This occurs when you have tunable parameters in Constant blocks that are connected to enabled subsystems or the trigger input of Switch blocks. In these situations, configure Simulink Design Verifier parameter support as described in Chapter 5, “Specifying Parameter Configurations”.

Modifying the Analysis Parameters

If the analysis satisfied most but not all of the objectives, try the following steps:

- 1 Increase the **Maximum analysis time** parameter. Such an increase gives the analysis more time to satisfy all the objectives.
- 2 Set the **Model coverage objectives** parameter to **Decision**. Selecting this option generates only test cases that achieve decision coverage. These test cases are a subset of the **MCDC** option.
- 3 Rerun the analysis and review the report.

If the results are not satisfactory, try the techniques described in the following sections.

Using the Large Model Optimization

Set the **Test suite optimization** parameter to `Large model`, and rerun the Simulink Design Verifier analysis.

The large model optimization strategy is designed for large, complex models. It may or may not improve the results of your analysis enough to fully test your design.

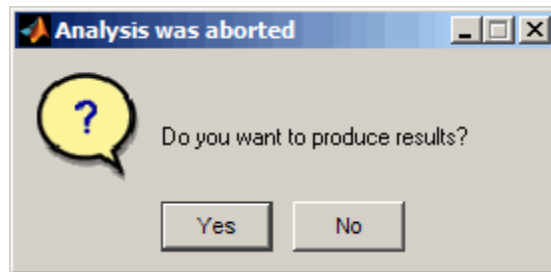
If there are outstanding test cases you want the software to generate, or additional properties you need to prove, continue with the following techniques.

Stopping the Analysis Before Completion

Watch the **Objectives processed** value in the log window. If about 50 percent of the **Maximum analysis time** parameter has elapsed and this value does not increase, the model analysis may have trouble processing certain objectives. If the analysis does not progress, take the following steps:

- 1 Click **Stop** in the log window.

The following dialog box opens.



- 2 Click **Yes** to save the results.

The software creates a test harness and an HTML report.

- 3 Review the results. In the HTML report, review the **Objectives Undecided when the Analysis was Stopped** and **Objectives Producing Errors** sections to identify the model elements that are causing problems.

- 4** Review the model elements that have undecided objectives or objectives with errors to see if any of the following problems are present. Consult the respective sections for specific techniques to improve the analysis:
- Floating-point inputs
See “Managing Model Data to Simplify the Analysis” on page 10-9.
 - Nonlinear operations
See “Analyzing the Model Using a Bottom-Up Approach” on page 10-15 and “Analyzing Logical Operations” on page 10-16.
 - Large state spaces
See “Handling Models with Large State Spaces” on page 10-17.
 - Large timers and time delays
See “Handling Problems with Counters and Timers” on page 10-18.

Generating Reports for Large Models

When you analyze a model with a large root-level input signal count, you may encounter an insufficient memory error when the Simulink Design Verifier software is generating the report.

When this occurs, you need to increase the amount of memory the Sun Java Virtual Machine (JVM™) software can allocate. For steps on how to increase this memory, see “Increasing the MATLAB JVM Memory Allocation Limit” in the MATLAB® Report Generator™ documentation.

Managing Model Data to Simplify the Analysis

In this section...
“Simplifying Data Types” on page 10-9
“Constraining Data” on page 10-9

Simplifying Data Types

One way to simplify your model is to use for the designated signal data type a data type requiring the smallest space for the expected data. For example, do not use an `int` data type for Boolean data, because only 1 bit is required for Boolean data.

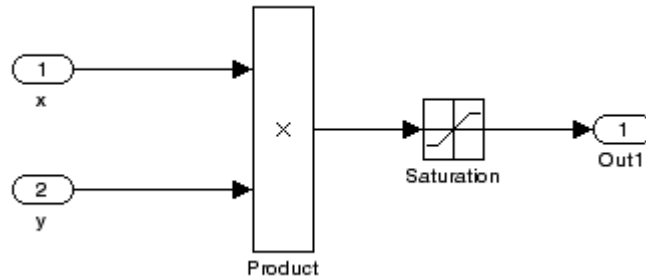
In another example, suppose you have a Sum block with two inputs that are always going to be integers between -10 and 10 . In this example, set the **Output data type** parameter to `int8`, rather than `int32` or `double`, or any other data type that requires more space than necessary.

To display the signal data types in the model window, select **Format > Port/Signal Displays > Port Data Types**.

Constraining Data

Another effective technique for reducing complexity is to restrict the inputs to a set of representative values or, ideally, a single constant value. This process, called *discretization*, treats the input as if it were an enumeration. Discretization allows you to handle nonlinear arithmetic from multiplication and division in the simplest way possible.

The following model has a Product block feeding a Saturation block.

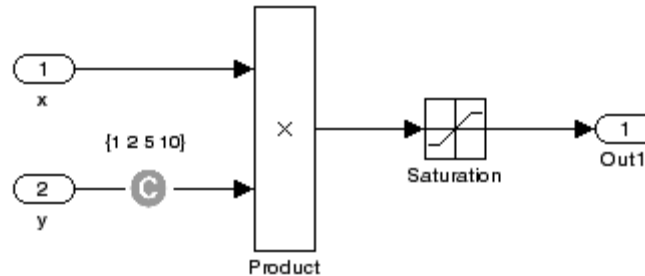


The Simulink Design Verifier software generates errors when attempting to satisfy the upper and lower limits of the Saturation block, because the software does not support nonlinear arithmetic. To work around these errors, restrict one of the inputs to a set of discrete values.

Identify discrete values that are required to satisfy your testing needs. For example, you may have an input for model speed, and your design contains paths of execution that are conditioned on speed above or below thresholds of 80, 150, 600, and 8000 RPM. For an effective analysis, constrain speed values to be 50, 100, 200, 1000, 5000, or 10000 RPM so that every threshold can be either active or inactive.

If you need to use more than two or three values, consider specifying the constrained values using an expression like `num2cell(minval:increment:maxval)`.

Using the previous example model, restrict the second input (*y*) to be either 1, 2, 5, or 10 using the Test Condition block as shown. The Simulink Design Verifier software produces test cases for all inputs.



You can also constrain signals that are intermediate or output values of the model. Constraining such signals makes it easier to work around multiplication or divisions inside lower-level subsystems that do not depend on model inputs.

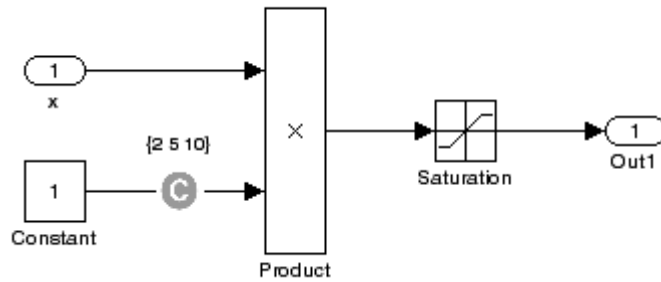
Note Discretization is best limited to a small number of inputs (less than 10). If your model requires discretization of many inputs, try to achieve model coverage through successive simulations as described in “Partitioning Model Inputs and Generating Tests Incrementally” on page 10-13.

Test Condition blocks do not need to be placed exactly on the inputs. In deciding where to place the constraints in your model, consider the following guidelines:

- Favor constraints on the input values because the software can process inputs easier.
- If you need to place constraints on both the input and the output, for example, to avoid nonlinear arithmetic, one of the constraints should be a range such as [minval maxval]. The software first tests the values at both ends of the range and can return a test case, even if the underlying calculations are nonlinear.
- Make sure that constraints at corresponding input and output points are not contradictory. Do not constrain the output signals to values that are not achievable because of the constraints on the input values.

- Avoid creating constraints that contradict the model. Such contradictions occur when a constraint can never be satisfied because it contradicts some aspect of the model or another constraint. Analyzing contradictory models can cause the Simulink Design Verifier software to hang.

The next figure shows a simple example of a contradictory model. The second input to the Multiply block is the constant 1, but the Test Condition block constrains it to a value of 2, 5, or 10. The software cannot achieve all the test objectives in this model.



- When you work with large models that have many multiplication and division operations, you may find it easier to add constraints to all of the floating-point inputs rather than to identify the precise set of inputs that require constraints.

Partitioning Model Inputs and Generating Tests Incrementally

As described in “Constraining Data” on page 10-9, you can constrain the values of model inputs using the Simulink Design Verifier Test Condition block.

Like other Simulink parameters, constraint values can be shared across several blocks by referencing a common workspace variable, and they can be initialized from M-files. If you have several inputs related to speed, such as desired speed, measured speed, and average speed, you might choose to constrain all of them to the same set of values.

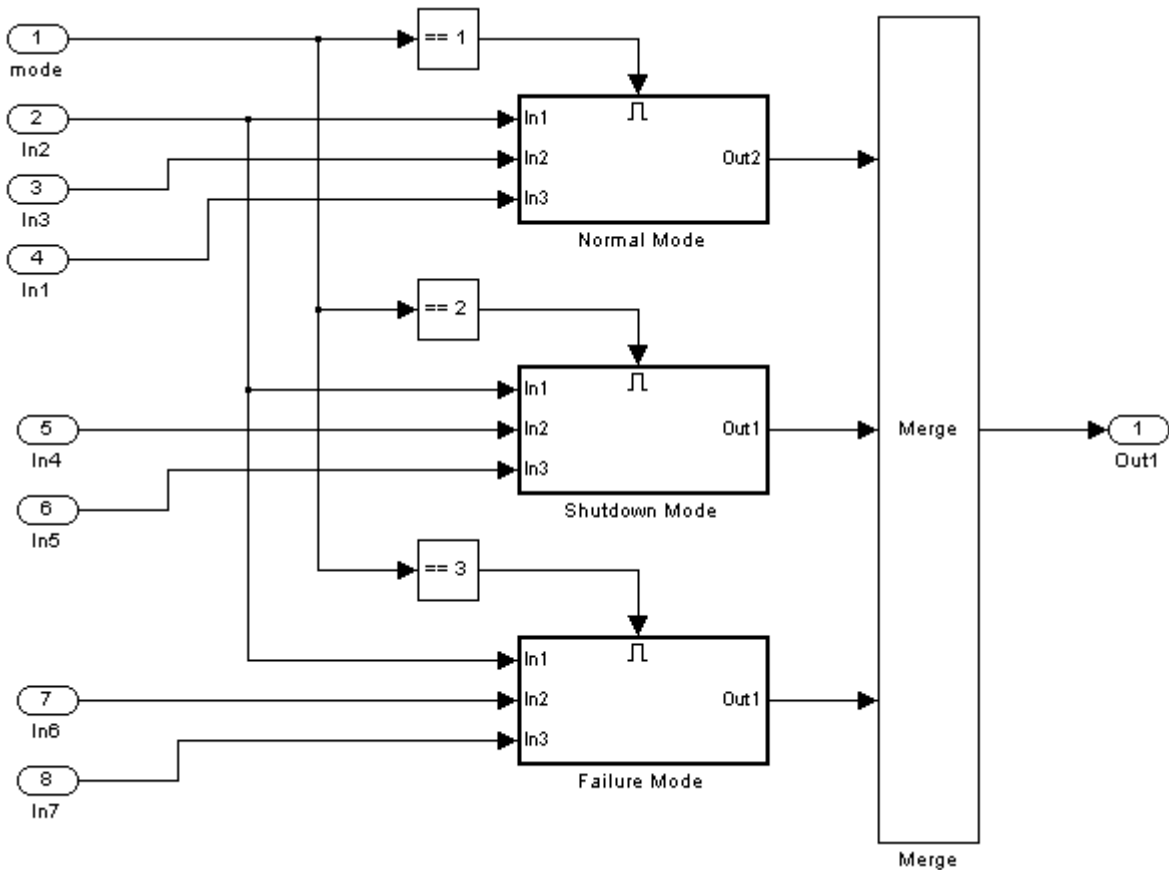
As an advanced technique for experienced MATLAB programmers, you can use parameterized constraints and successive runs of the Simulink Design Verifier software to implement an incremental test-generation technique:

- 1** Partition model inputs so that some are held constant, some are constrained to sets of constants using the Test Condition block, and some are free.
- 2** Generate test cases and run those test cases to collect model coverage.
- 3** Choose new values and partition the inputs with these new values.
- 4** Generate test cases for missing coverage using `sldvgencov` and the current test coverage.

Note The Extending an Existing Test Suite demo shows how to extend a test suite so that it satisfies missing model coverage.

- 5** Repeat steps 3 and 4 until you have generated sufficient coverage.

Partition the model inputs that enable further simplification when an analysis runs. Consider the following model, which has three mutually independent enabled subsystems—Normal Mode, Shutdown Mode, and Failure Mode.



You can incrementally generate test cases for each subsystem by constraining the first input to the appropriate constant value before running an analysis. In this way, as you create test cases for each subsystem, the software ignores the complexity of the other two subsystems.

Analyzing the Model Using a Bottom-Up Approach

Simulink Design Verifier software works most effectively at analyzing large models using a bottom-up approach. In this approach, the software analyzes smaller model components first, which can be faster than using the Large model test suite optimization.

The bottom-up approach offers several advantages:

- It allows you to solve the problems that slow down test generation or property proving in a controlled environment.
- Solving problems with small model components before analyzing the model as a whole is more efficient, especially if you have unreachable components in your model that you can only discover in the context of the model.
- You can iterate more quickly—find a problem and fix it, find another problem and fix it, and so on.
- If one model component has a problem, for example, it's unreachable, that situation can prevent the software from generating tests for *all* the objectives in a large model.

Try this workflow with your large model:

- 1** Break down the model into components of 100–1000 objectives each. Use the `sldvextract` function to extract components into a new model for analysis purposes.
- 2** Analyze the individual components, starting with the lowest level subsystems.
- 3** Fix any problems by adding constraints or specifying block replacements.
- 4** After you analyze the smaller components, reapply the necessary constraints and substitutions to the original model and analyze the full model.

When you finish a bottom-up analysis, you should have a top-level model that the Simulink Design Verifier software can analyze quickly.

Analyzing Logical Operations

If you have a model with both logical and arithmetic operations, consider analyzing only the logical operations.

The Simulink Design Verifier software does not support nonlinear arithmetic of floating-point numbers, as occurs with multiplication or division, unless one of the multiply operands or the divisor is a constant.

To simplify models that contain integers or floating-point numbers, the software maps the model computations into expressions of Boolean variables. For example, the software might represent an 8-bit number as a set of 8 Boolean values, with one for each digit. It might represent a bitwise OR operation of two 8-bit integers as 8 separate logical OR operations.

Mapping problems of one data type into Boolean variables is complex, and this complexity increases when the software performs such mapping. The software handles models with predominantly logical signals more efficiently than it does those with large integer or floating-point signals.

Note Simulink Design Verifier software can handle floating-point inputs when their values impact the design through linear inequalities such as $x < y$ or $a > 0$.

In addition, input complexity can result from certain cast operations. For example, casting a `double` to an `int8` can introduce a nonlinearity in certain situations.

Handling Models with Large State Spaces

Persistent design variables (variables that are assigned in one time step and used in a later time step during simulation) affect the complexity of analysis in much the same way as input complexity. You can use one or more of the following techniques to simplify the complexity of the state space you want to search:

- Apply constraints to input signals that are delayed.
- Constraint the inputs to states that are contained within conditionally executed subsystems.
- Limit the number of test case steps by setting the **Maximum test case step** parameter to 20.
- Increase the sample time for part or all of the model. (This procedure is similar to reducing timer thresholds, as described in “Handling Problems with Counters and Timers” on page 10-18.) A test case you generate at a lower sample rate often has similarities to the test case with a high sample rate that you need to achieve an objective.

States that are computed from previous state values present a special challenge. For example, if you want to restrict the integrator value in a PID controller, you can only use a set of values that includes all reachable values from the initial value. Otherwise, the input must be forced to 0. Neither of these limitations is practical and would probably make test generation or property proving less complete.

Alternatively, you can use any existing simulation data to help satisfy your testing needs. If you have existing test data, run it on your model and collect model coverage. By using the `sldvgen cov` function, you can ignore model coverage objectives that have already been satisfied in simulation when you supply a coverage data object.

Note For more information on satisfying missing model coverage, see the [Extending an Existing Test Suite](#) demo.

Handling Problems with Counters and Timers

Complexity from states occurs from both the size of the state representation and the number of time steps required to transition from one state to another. The Simulink Design Verifier software searches through sequences of time steps, starting from the default configuration, to find input values that reach a state that satisfies an objective.

Note For the purposes of Simulink Design Verifier analysis, the term *configuration* refers to a set of values for all the persistent information in your model.

The search process investigates all configurations that can be reached in a single time step before considering any of the configurations that can be reached in two time steps. Likewise, the search investigates all configurations that can be reached in two time steps before it considers any configuration that requires three or more time steps, etc.

Models that contain time delays, such as countdown timers, hinder the analysis by forcing the search to span large numbers of time steps. By design, the value of a counter can reach n only when its previous value is $n - 1$.

You may see similar effects when systems use extensive averaging and filtering to delay the response to a change in inputs. Any aspect of the design that delays the response causes the test sequences to contain more time steps, resulting in longer test cases that are more difficult to identify.

Some basic techniques you can use to improve performance in models that have delays include:

- 1 Make time delays tunable parameters. Choose very small values when running a Simulink Design Verifier analysis. A system with a logical error when a time delay is set to 2000 steps usually demonstrates that error if the time delay is changed to 2 steps. If your system has several delays, choose small but unique values for each of them so that your delays are progressively satisfied.

- 2** Choose higher-frequency cutoffs for filters and fewer samples to average to minimize filtering delays.
- 3** Make the initial values of counters and timers parameter values that the Simulink Design Verifier software can modify. The software finds initial values that allow shorter test cases to exceed thresholds.

Techniques for Proving Properties of Large Models

Property proving uses the same underlying techniques as test generation and suffers from the same performance limitations. However, unlike test generation, you often cannot simplify the problem without compromising the validity of the results.

You can quickly prove simple proof objectives that are not affected by model dynamics. However, a successful proof requires that the Simulink Design Verifier software search through all reachable configurations of your model—even the ones that are reached only after long time delays. The computation time and memory required to search a model completely often make an exhaustive proof impractical.

Simulink Design Verifier software offers a bounded model-checking capability to examine properties in larger, more complicated models. Bounded model checking restricts the search for property violations to a predefined limit of time steps. If a violation is not detected, it is impossible to violate the property with any input sequence having fewer time steps than the specified limit. However, you cannot prove that the property is true because there might be a counterexample within more time steps than the specified limit.

To configure the software for bounded model checking, on the **Design Verifier > Property Proving** pane of the Configuration Parameters dialog box, specify the value of the **Strategy** parameter as **Find violation**. When you use this strategy, the **Maximum violation steps** parameter becomes active so that you can specify an upper bound for the number of time steps in the search.

Note For more information about the parameters for property proving, see “Property Proving Pane” on page 6-12.

Use the following technique for proving properties in large model combines proving and searching for violations:

- 1 On the **Design Verifier > Property Proving** pane, set the **Strategy** parameter to **Prove**.

- 2** On the **Design Verifier** pane, use a relatively short value for the **Maximum analysis time** parameter, such as 5–10 minutes. If there are trivial counterexamples—or if your properties do not depend on model dynamics—the analysis should complete in that amount of time.
- 3** Change the **Strategy** parameter to **Find violation**, and choose a small bound for the **Maximum violation steps** parameter, such as 4, 5, or 6. If your properties have simple counterexamples, the software should discover them.
- 4** If you do not find any violations with a small bound, increase the bound and look for longer counterexamples.
 - a** Increase the bound in several increments, and observe the processing time and memory consumption. System resources might limit the length of violation that can be searched.
 - b** In addition, consider the dynamics of your model and the number of time steps needed to transition between an arbitrary pair of configurations. If you choose too large a bound, the violation search can be more complex than the unbounded proof.
- 5** If you can run violation searches with relatively large bounds, e.g., 30–50 time steps, switch back to the **Prove** strategy, and use a longer time limit, such as several hours.

Function Reference

sldvblockreplacement

Purpose Replace model blocks to support Simulink Design Verifier analysis

Syntax

```
[status, newmodel] = sldvblockreplacement(model)
[status, newmodel] = sldvblockreplacement(model, options)
[status, newmodel] = sldvblockreplacement(model, options,
    showUI)
```

Description

[status, newmodel] = sldvblockreplacement(model) copies the open model and replaces specified model blocks and other model components to prepare the model for a Simulink Design Verifier analysis. sldvblockreplacement replaces the blocks of the model according to the block replacement rules specified in the configuration settings associated with model, and returns a handle to the new model in newmodel. sldvblockreplacement returns 1 upon successful completion. Otherwise, it returns 0.

[status, newmodel] = sldvblockreplacement(model, options) replaces the blocks of the open model according to the block replacement rules using the sldvoptions object specified by options, and returns a handle to the new model in newmodel.

[status, newmodel] = sldvblockreplacement(model, options, showUI) performs the same tasks as sldvblockreplacement(model, options). If you set showUI to false (the default), any errors appear at the MATLAB command line; if you set showUI to true, any errors appear in the Simulation Diagnostics Viewer.

See Also sldvoptions

Purpose Check model for compatibility with Simulink Design Verifier analysis

Syntax

```
status = sldvcompat(model)
status = sldvcompat(block)
status = sldvcompat(model, options)
```

Description `status = sldvcompat(model)` returns 1 if the open model is compatible with the Simulink Design Verifier software; otherwise, it returns 0. When checking for compatibility, if you select the **Apply block replacements** parameter, the Simulink Design Verifier software replaces model blocks

Note If you call this function without specifying a model, the function operates on the current open model.

`status = sldvcompat(block)` converts the Simulink block into a temporary model, and then checks the compatibility of that model with the Simulink Design Verifier software. The function destroys the temporary model after the compatibility check.

`status = sldvcompat(model, options)` checks the subsystem specified by the open model for compatibility with the Simulink Design Verifier software using the `sldvoptions` object specified by `options`.

Examples The following commands open the `vdp` demo model and check for its compatibility with the Simulink Design Verifier software:

```
vdp
status = sldvcompat('vdp')
```

The Simulink Design Verifier software displays a result that indicates the vdp model is not compatible:

```
Checking compatibility of model "vdp"

Model "vdp" is not compatible with Simulink Design Verifier

status =

    0
```

The following commands open sldvdemo_flipflop and check for its compatibility with the Simulink Design Verifier software:

```
sldvdemo_flipflop
status = sldvcompat('sldvdemo_flipflop')
```

The Simulink Design Verifier software displays the results that indicate the sldvdemo_flipflop model is compatible:

```
Checking compatibility of model "sldvdemo_flipflop"

Compiling model...done
Checking compatibility...done

Model "sldvdemo_flipflop" is compatible with
    Simulink Design Verifier.

ans =

    1
```

See Also

sldvoptions, sldvrun

Purpose	Extract subsystem contents into new model for Simulink Design Verifier analysis
Syntax	<pre>[status, modelH] = sldvextract(blockH) [status, modelH] = sldvextract(blockH, showModel) [status, modelH] = sldvextract(blockH, showModel, showUI) [status, modelH] = sldvextract(blockH, showModel, showUI, isvalid)</pre>
Description	<p>[status, modelH] = sldvextract(blockH) extracts the contents of the subsystem that blockH specifies and creates a new model that you can analyze using the Simulink Design Verifier software. The sldvextract function returns the handle of the new model in modelH. It returns status as 1 upon successful completion; otherwise, it returns 0.</p> <p>[status, modelH] = sldvextract(blockH, showModel) opens the extracted model if you set showModel to true.</p> <p>[status, modelH] = sldvextract(blockH, showModel, showUI) performs the same tasks as sldvextract(blockH, showModel, showUI). If you set showUI to false (the default), any errors appear at the MATLAB command line; if you set showUI to true, any errors appear in the Simulation Diagnostics Viewer.</p> <p>[status, modelH] = sldvextract(blockH, showModel, showUI, isvalid) performs the same tasks as sldvextract(blockH, showModel, showUI). The isvalid arguments is reserved for internal use.</p>

sldvgencov

Purpose	Run Simulink Design Verifier analysis to obtain missing model coverage
Syntax	<pre>[status, cvdo] = sldvgencov(model, options, showUI, startCov) [status, cvdo] = sldvgencov(block, options, showUI, startCov)</pre>
Description	<p>[status, cvdo] = sldvgencov(model, options, showUI, startCov) runs a Simulink Design Verifier analysis on the model using the sldvoptions object options.</p> <p>[status, cvdo] = sldvgencov(block, options, showUI, startCov) runs an analysis on the atomic subsystem block using the sldvoptions object options.</p> <p>Set showUI to true to open the log window during analysis. Set showUI to false to direct output to the MATLAB command line.</p> <p>The analysis ignores all model coverage objectives that are satisfied in the cvdata object specified by startCov.</p> <p>sldvgencov returns 1 for status if the Simulink Design Verifier software was successful; otherwise, it returns 0. It also measures the coverage in the new tests and returns the resulting cvdata object cvdo.</p>
See Also	sldvoptions, sldvrun

Purpose Merge test cases and initializations into one model

Syntax `status = sldvharnessmerge(name, models,
initialization_commands)`

Description `status = sldvharnessmerge(name, models, initialization_commands)` collects the test data and initialization commands from each test harness model listed in `models` and saves them in `name`. This function assumes that you have created each test harness model with the Simulink Design Verifier software, either with the `sldvrun` function or the **Tools > Design Verifier > Generate Tests** menu item.

If `name` does not exist, this function creates it as a copy of the model in `models`. `sldvharnessmerge` then copies the data from the other models into this model. If `name` was created from a previous `sldvharnessmerge` run, subsequent runs of this function for `name` maintain the correct structure and initialization from that earlier run. If `name` matches an existing Simulink model, this function merges the test data from `models` into `name`.

- `models` can be a cell array of model names or an array of model handles.
- `initialization_commands` must be a cell array of strings the same length as `models`. `initialization_commands` define parameter settings for the test cases of each test harness model. Each time a model test case executes, the associated initialization command is evaluated in the base workspace.

Consider using `sldvharnessmerge` with `sldvgencov` to combine test cases that use different sets of parameter values.

See Also `sldvgencov`

sldvisactive

Purpose Check if Simulink Design Verifier software is analyzing model

Syntax

```
status = sldvisactive
status = sldvisactive(model)
status = sldvisactive(block)
```

Description

`status = sldvisactive` checks if the Simulink Design Verifier software is actively analyzing the current Simulink model.

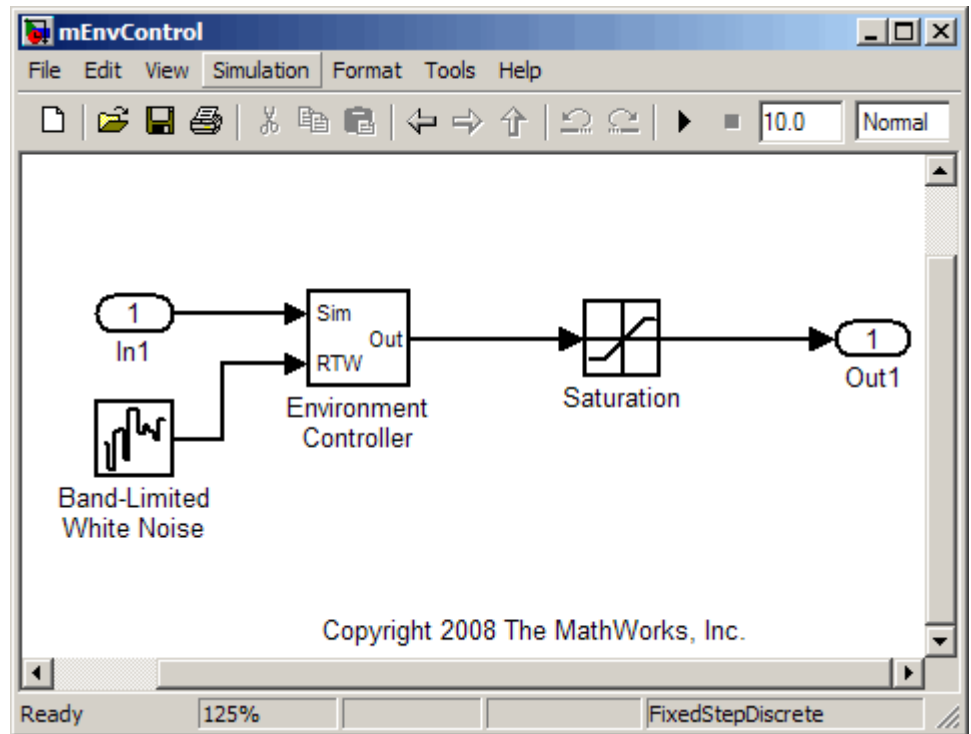
`status = sldvisactive(model)` checks if the Simulink Design Verifier software is actively analyzing the model, `model`.

`status = sldvisactive(block)` checks to see if the Simulink Design Verifier software is actively analyzing the model that contains the block, `block`.

Use the `sldvisactive` function in block callback functions, model callback functions, or mask initialization to customize the analysis of the model. For example, you can use `sldvisactive` to eliminate any blocks that are incompatible with the Simulink Design Verifier software.

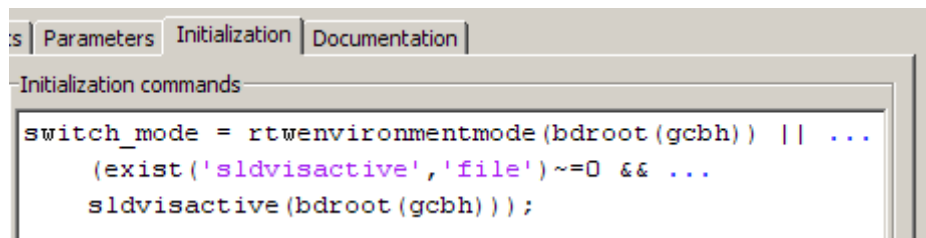
Output `sldvisactive` returns 1 if Simulink Design Verifier is active, otherwise, it returns 0.

Example In the `mEnvControl` model shown in the following graphic, the mask initialization of the Environment Controller block calls `sldvisactive`.



The Simulink Design Verifier software does not support Band-Limited White Noise blocks. If the software is analyzing the `mEnvControl` model, the mask initialization of the Environment Controller block sets the pass-through mode to pass the Sim signal to the output port and eliminate the RTW port, which is incompatible with the Simulink Design Verifier software.

sldvisactive



The screenshot shows a software interface with three tabs: "Parameters", "Initialization", and "Documentation". The "Initialization" tab is selected, and the text "Initialization commands" is visible above a code editor. The code editor contains the following MATLAB code:

```
switch_mode = rtwenvironmentmode (bdroot (gcbh)) || ...  
    (exist ('sldvisactive', 'file') ~= 0 && ...  
    sldvisactive (bdroot (gcbh)) );
```

Purpose Access Simulink Design Verifier options object

Syntax
`options = sldvoptions`
`options = sldvoptions(model)`

Description `options = sldvoptions` returns a Simulink Design Verifier options object that contains default values for its parameters (described in this section).

`options = sldvoptions(model)` returns the Simulink Design Verifier options object attached to the open `model`.

sldvoptions Object Parameters The following table describes the parameters that comprise a Simulink Design Verifier options object.

Parameter	Description	Values
Assertions	Set by the Assertion blocks option on the Design Verifier > Property Proving pane of the Configuration Parameters dialog box.	'EnableAll' 'DisableAll' {'UseLocalSettings'}
AutomaticStubbing	Set by the Automatic stubbing of unsupported blocks and functions option on the Design Verifier pane of the Configuration Parameters dialog box.	'on' {'off'}

sldvoptions

Parameter	Description	Values
BlockReplacement	Set by the Apply block replacements option on the Design Verifier > Block Replacements pane of the Configuration Parameters dialog box.	'on' {'off'}
BlockReplacementModel-FileName	Set by the File path of the output model option on the Design Verifier > Block Replacements pane of the Configuration Parameters dialog box.	string {'\$ModelName\$_replacement'}
BlockReplacementRules-List	Set by the List of block replacement rules option on the Design Verifier > Block Replacements pane of the Configuration Parameters dialog box.	string {'<FactoryDefaultRules>'}
DataFileName	Set by the Data file name option on the Design Verifier > Results pane of the Configuration Parameters dialog box.	string {'\$ModelName\$_sldvdata'}
DisplayReport	Set by the Display report option on the Design Verifier > Report pane of the Configuration Parameters dialog box.	{'on'} 'off'

Parameter	Description	Values
DisplayUnsatisfiableObjectives	Set by the Display unsatisfiable test objectives option on the Design Verifier pane of the Configuration Parameters dialog box.	{'on'} 'off'
HarnessModelFileName	Set by the Harness model file name option on the Design Verifier > Results pane of the Configuration Parameters dialog box.	string {'\$modelName\$_harness'}
MakeOutputFilesUnique	Set by the Make output file names unique by adding a suffix check box on the Design Verifier pane of the Configuration Parameters dialog box.	{'on'} 'off'
MaxProcessTime	Set by the Maximum analysis time option on the Design Verifier pane of the Configuration Parameters dialog box.	double {'600'}
MaxTestCaseSteps	Set by the Maximum test case steps option on the Design Verifier > Test Generation pane of the Configuration Parameters dialog box.	int32 {'500'}

sldvoptions

Parameter	Description	Values
MaxViolationSteps	Set by the Maximum violation steps option on the Design Verifier > Property Proving pane of the Configuration Parameters dialog box.	int32 {'20'}
Mode	Set by the Mode option on the Design Verifier pane of the Configuration Parameters dialog box.	{'TestGeneration'} 'PropertyProving'
ModelCoverageObjectives	Set by the Model coverage objectives option on the Design Verifier > Test Generation pane of the Configuration Parameters dialog box.	'None' 'Decision' 'ConditionDecision' {'MCDC'}
ModelReferenceHarness	Set by the Reference input model in generated harness option on the Design Verifier > Results pane of the Configuration Parameters dialog box.	'on' {'off'}
OutputDir	Set by the Output directory option on the Design Verifier pane of the Configuration Parameters dialog box.	string {'sldv_output/\$ModelName\$'}

Parameter	Description	Values
Parameters	Set by the Apply parameters option on the Design Verifier > Parameters pane of the Configuration Parameters dialog box.	{'on'} {'off'}
ParametersConfigFile-Name	Set by the Parameter configuration file option on the Design Verifier > Parameters pane of the Configuration Parameters dialog box.	string {'sldv_params_template.m'}
ProofAssumptions	Set by the Proof assumptions option on the Design Verifier > Property Proving pane of the Configuration Parameters dialog box.	'EnableAll' 'DisableAll' {'UseLocalSettings'}
ProvingStrategy	Set by the Strategy option on the Design Verifier > Property Proving pane of the Configuration Parameters dialog box.	'FindViolation' {'Prove'} 'ProveWithViolationDetection'
RandomizeNoEffectData	Set by the Randomize data that does not affect outcome option on the Design Verifier > Results pane of the Configuration Parameters dialog box.	'on' {'off'}

sldvoptions

Parameter	Description	Values
ReportFileName	Set by the Report file name option on the Design Verifier > Report pane of the Configuration Parameters dialog box.	string {'\$ModelName\$_report'}
ReportIncludeGraphics	Set by the Include screen shots of properties and test objectives option on the Design Verifier > Report pane of the Configuration Parameters dialog box.	'on' {'off'}
SaveDataFile	Set by the Save test data to file option on the Design Verifier > Results pane of the Configuration Parameters dialog box.	{'on'} 'off'
SaveExpectedOutput	Set by the Include expected output values option on the Design Verifier > Results pane of the Configuration Parameters dialog box.	'on' {'off'}
SaveHarnessModel	Set by the Save test harness as model option on the Design Verifier > Results pane of the Configuration Parameters dialog box.	{'on'} 'off'

Parameter	Description	Values
SaveReport	Set by the Generate report of the results option on the Design Verifier > Report pane of the Configuration Parameters dialog box.	{'on'} {'off'}
SaveSystemTestHarness	Set by the Save test harness as SystemTest TEST-File option on the Design Verifier > Results pane of the Configuration Parameters dialog box.	'on' {'off'}
SystemTestFileName	Set by the SystemTest file name option on the Design Verifier > Results pane of the Configuration Parameters dialog box.	\$ModelName\$_harness
TestConditions	Set by the Test conditions option on the Design Verifier > Test Generation pane of the Configuration Parameters dialog box.	'EnableAll' 'DisableAll' {'UseLocalSettings'}

sldvoptions

Parameter	Description	Values
TestObjectives	Set by the Test objectives option on the Design Verifier > Test Generation pane of the Configuration Parameters dialog box.	'EnableAll' 'DisableAll' {'UseLocalSettings'}
TestSuiteOptimization	Set by the Test suite optimization option on the Design Verifier > Test Generation pane of the Configuration Parameters dialog box.	{'CombinedObjectives'} 'IndividualObjectives' 'LargeModel' 'LongTestCases'

See Also

sldvblockreplacement, sldvcompat, sldvgencov, sldvrun

Purpose Run Simulink Design Verifier analysis on model or subsystem

Syntax

```
status = sldvrun(model)
status = sldvrun(block)
status = sldvrun(model, options)
[status, filenames] = sldvrun(model, options)
[status, filenames] = sldvrun(model, options, showUI,
    startCov)
```

Description `status = sldvrun(model)` runs a Simulink Design Verifier analysis on the specified `model`. The Simulink Design Verifier software uses the configuration settings associated with `model` (if available). Otherwise, the software uses its default configuration settings. Upon completion, `sldvrun` returns one of the following values for `status`:

- -1 — Maximum processing time was exceeded.
- 0 — An error occurred.
- 1 — Preprocessing completed normally.

Note If you call this function without specifying a model, the function operates on the current system.

`status = sldvrun(block)` converts the Simulink `block` into a new model, and then runs a Simulink Design Verifier analysis on the new model. The Simulink Design Verifier software uses the configuration settings associated with the parent model of `block` (if available). Otherwise, the software uses its default configuration settings.

`status = sldvrun(model, options)` runs a Simulink Design Verifier analysis on the model specified by `model`. The Simulink Design Verifier software uses the `sldvoptions` object specified by `options`.

`[status, filenames] = sldvrun(model, options)` runs a Simulink Design Verifier analysis on the model specified by `model`. This function

returns `status` and `filenames`, a structure whose fields list the names of the files that the Simulink Design Verifier software generates:

- `DataFile` — MAT-file that contains raw input data
- `HarnessModel` — Simulink harness model
- `SystemTestFile` — SystemTest TEST-file
- `Report` — HTML report that documents the results
- `ExtractedModel` — Simulink model extracted from subsystem
- `BlockReplacementModel` — Simulink model obtained after block replacements

`[status, filenames] = sldvrun(model, options, showUI, startCov)` opens the log window during analysis if you set `showUI` to `true`. If you set `showUI` to `false` (the default), it directs output to the MATLAB command line. The analysis ignores all model coverage objects that are satisfied in the `cvdata` object specified by `startCov`.

See Also

`sldvcompat`, `sldvgencov`, `sldvoptions`

Purpose

Simulate model using test case in Simulink Design Verifier data file

Syntax

```
data = sldvrntest(model, sldvDataFile, testIdx)
data = sldvrntest(model, sldvDataFile)
[data, cvdo] = sldvrntest(model, sldvDataFile, testIdx,
    true)
[data, cvdo] = sldvrntest(model, sldvDataFile, [], true)
[data, cvdo] = sldvrntest(model, sldvDataFile, testIdx, cvt)
[data, cvdo] = sldvrntest(model, sldvDataFile, [], cvt)
[data, cvdo] = sldvrntest(model, sldvDataFile, testIdx, true,
    outputFormat)
```

Description

`data = sldvrntest(model, sldvDataFile, testIdx)` simulates `model` using input signals associated with a single test case that the Simulink Design Verifier software generated. `testIdx` specifies the index of the test case that the `sldvDataFile` MAT-file contains. This function returns `data`, a structure whose fields contain the simulation results:

- `T` — Simulation time vector
- `X` — Simulation state matrix
- `Y` — Simulation output captured in time-series objects or, if the Output block specifies a bus object, in time-series array objects

`data = sldvrntest(model, sldvDataFile)` simulates `model` using all test cases that the MAT-file `sldvDataFile` contains. For each test case, the software uses the stop time associated with that particular test case.

`[data, cvdo] = sldvrntest(model, sldvDataFile, testIdx, true)` simulates `model` using the test case that `testIdx` indexes in the MAT-file `sldvDataFile`. The Simulink Verification and Validation software collects model coverage information during the simulation, which the function returns in the `cvdata` object `cvdo`.

`[data, cvdo] = sldvrntest(model, sldvDataFile, [], true)` simulates `model` using all test cases in the MAT-file, `sldvDataFile`.

sldvruntest

The Simulink Verification and Validation software collects model coverage information during the simulation, which the function returns in the `cvdata` object `cvdo`.

`[data, cvdo] = sldvruntest(model, sldvDataFile, testIdx, cvt)` runs a simulation using the test case that `testIdx` indexes in the MAT-file `sldvDataFile`, and records coverage data. The coverage tool uses the settings in the `cvtest` object `cvt`.

`[data, cvdo] = sldvruntest(model, sldvDataFile, [], cvt)` runs simulations for each test case and records the cumulative coverage. The coverage tool uses the settings in the `cvtest` object `cvt`.

`[data, cvdo] = sldvruntest(model, sldvDataFile, testIdx, true, outputFormat)` stores the output values of the model in `Y` in the `structuredata`. If you set `outputFormat` to `'Timeseries'` (the default), the output values are stored in the `Timeseries` format. If you set `outputFormat` to `'StructureWithTime'` and the model's output signals do not include bus signals, the output values are stored in the `Structure with time` format.

See Also

`cvsim` (in the *Simulink Verification and Validation User's Guide*), `sim` (in the *Simulink Reference*)

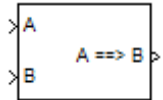
Block Reference

Implies

Purpose Specify conditions that produce response

Library Simulink Design Verifier

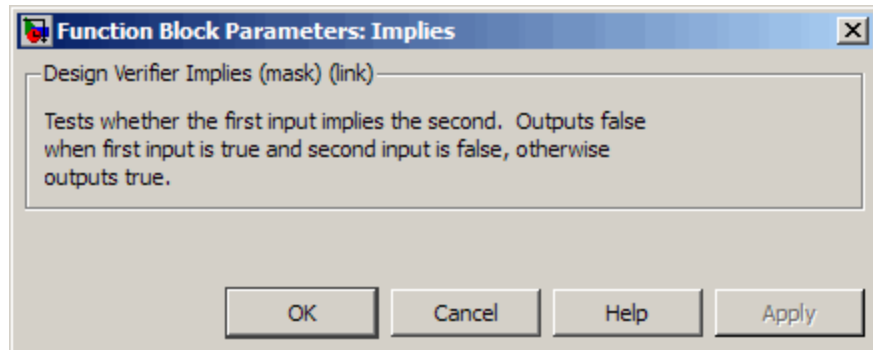
Description



The Implies block lets you specify conditions to produce a given response, for example, when you press the brake pedal on a car, the cruise control mechanism becomes disabled. If input A is true and input B is false, the output is false; for all other pairs of inputs, the output is true.

You can use the Implies block in any model, not just when you run the Simulink Design Verifier software.

Parameters and Dialog Box



Purpose

Constrain signal values when proving model properties

Library

Simulink Design Verifier

Description



When operating in property-proving mode, the Simulink Design Verifier software proves that properties of your model satisfy specified criteria (see Chapter 8, “Proving Properties of a Model”). In this mode, you can use Proof Assumption blocks to define assumptions for signals in your model. The **Values** parameter lets you specify constraints on signal values during a property proof. The block applies the specified **Values** parameter to its input signal, and the Simulink Design Verifier software proves or disproves that the properties of your model satisfy specified criteria.

The block’s parameter dialog box also allows you to:

- Enable or disable the assumption.
- Specify that the block should display its **Values** parameter in the model editor.
- Specify that the block should display its output port.

Note The Simulink and Real-Time Workshop software ignore the Proof Assumption block during model simulation and code generation, respectively. The Simulink Design Verifier software uses the Proof Assumption block only when proving model properties.

Specifying Proof Assumptions

Use the **Values** parameter to constrain signal values in property proofs. Specify any combination of scalars and intervals in the form of a MATLAB cell array. (For information about cell arrays, see “Cell Arrays” in the MATLAB documentation.)

Proof Assumption

Tip If the **Values** parameter specifies only one scalar value, you do not need to enter it in the form of a MATLAB cell array.

Scalar values each comprise a single cell in the array, for example:

`{0, 5}`

A closed interval comprises a two-element vector as a cell in the array, where each element specifies an interval endpoint:

`{[1, 2]}`

Alternatively, you can specify scalar values using the `Sldv.Point` constructor, which accepts a single value as its argument. You can specify intervals using the `Sldv.Interval` constructor, which requires two input arguments, i.e., a lower bound and an upper bound for the interval. Optionally, you can provide one of the following strings as a third input argument that specifies inclusion or exclusion of the interval endpoints:

- `'()'` — Defines an open interval.
- `'[]'` — Defines a closed interval.
- `'(]'` — Defines a left-open interval.
- `'][)'` — Defines a right-open interval.

Note By default, `Sldv.Interval` considers an interval to be closed if you omit its third input argument.

As an example, the **Values** parameter

`{0, [1, 3]}`

specifies:

- 0 — a scalar
- [1, 3] — a closed interval

The **Values** parameter

```
{Sldv.Interval(0, 1, '[') }, Sldv.Point(1)}
```

specifies:

- `Sldv.Interval(0, 1, '[')` — the right-open interval [0, 1)
- `Sldv.Point(1)` — a scalar

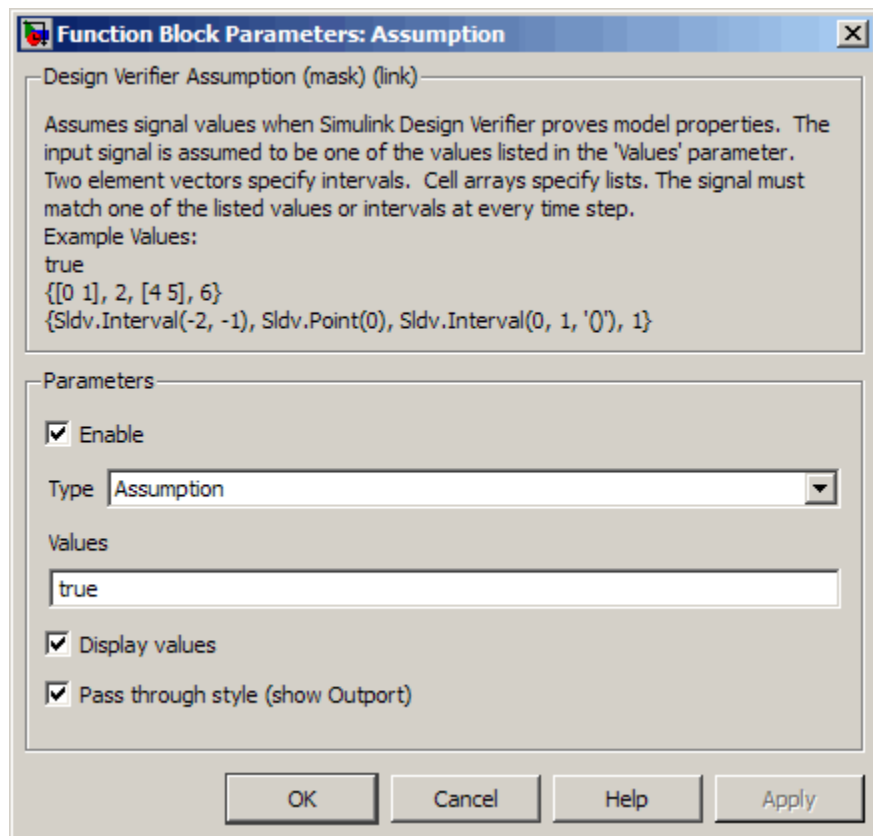
If you specify multiple scalars and intervals for a Proof Assumption block, the Simulink Design Verifier software combines them using a logical OR operation during the property proof. In this case, the software considers the entire assumption to be satisfied if any single scalar or interval is satisfied.

Data Type Support

The Proof Assumption block accepts signals of all built-in data types supported by the Simulink software. For a discussion on the data types supported by the Simulink software, see “Data Types Supported by Simulink” in *Simulink User’s Guide*.

Proof Assumption

Parameters and Dialog Box



Enable

Specify whether the block is enabled. If selected (the default), the Simulink Design Verifier software uses the block when proving properties of a model. Clearing this option disables the block, that is, causes the Simulink Design Verifier software to behave as if the Proof Assumption block did not exist. If this option is not selected, the block appears grayed out in the model editor.

Type

Specify whether the block behaves as a Proof Assumption or Test Condition block. Select **Test Condition** to transform the Proof Assumption block into a Test Condition block.

Values

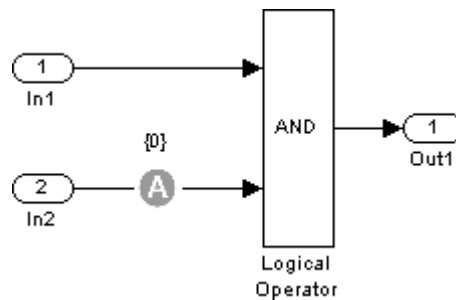
Specify the proof assumption (see “Specifying Proof Assumptions” on page 12-3).

Display values

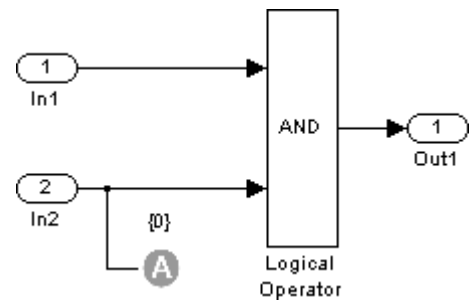
Specify whether the block displays the contents of its **Values** parameter in the model editor. By default, this option is selected.

Pass through style

Specify whether the block displays an output port in the model editor. If selected (the default), the block displays its output port, allowing its input signal to pass through as the block output. If not selected, the block hides its output port and terminates the input signal. The following figure illustrates the appearance of the block in each case.



Pass through style: selected



Pass through style: deselected

See Also

Proof Objective, Test Condition

Proof Objective

Purpose Define objectives that signals must satisfy when proving model properties

Library Simulink Design Verifier

Description When operating in property-proving mode, the Simulink Design Verifier software proves that properties of your model satisfy specified criteria (see Chapter 8, “Proving Properties of a Model”). In this mode, you can use Proof Objective blocks to define proof objectives for signals in your model.



The **Values** parameter lets you specify acceptable values for the block’s input signal. If a signal value deviates from the acceptable values in *any* time step, a property violation occurs and the proof objective is falsified. The block applies the specified **Values** parameter to its input signal, and the Simulink Design Verifier software proves or disproves that the properties of your model satisfy specified criteria.

The block’s parameter dialog box allows you to

- Enable or disable the objective.
- Specify that the block should display its **Values** parameter in the model editor.
- Specify that the block should display its output port.

Note The Simulink and Real-Time Workshop software ignore the Proof Objective block during model simulation and code generation, respectively. The Simulink Design Verifier software uses the Proof Objective block only when proving model properties.

Specifying Proof Objectives

Use the **Values** parameter to define values that a signal must achieve during a proof simulation. Specify any combination of scalars and intervals in the form of a MATLAB cell array. (For information about cell arrays, see “Cell Arrays” in the MATLAB documentation.)

Tip If the **Values** parameter specifies only one scalar value, you do not need to enter it in the form of a MATLAB cell array.

Scalar values each comprise a single cell in the array, for example:

```
{0, 5}
```

A closed interval comprises a two-element vector as a cell in the array, where each element specifies an interval endpoint:

```
{[1, 2]}
```

Alternatively, you can specify scalar values using the `Sldv.Point` constructor, which accepts a single value as its argument. You can specify intervals using the `Sldv.Interval` constructor, which requires two input arguments, i.e., a lower bound and an upper bound for the interval. Optionally, you can provide one of the following strings as a third input argument that specifies inclusion or exclusion of the interval endpoints:

- `'()'` — Defines an open interval.
- `'[]'` — Defines a closed interval.
- `'(]'` — Defines a left-open interval.
- `'[)'` — Defines a right-open interval.

Note By default, `Sldv.Interval` considers an interval to be closed if you omit its third input argument.

As an example, the **Values** parameter

```
{0, [1, 3]}
```

specifies:

Proof Objective

- 0 — a scalar
- [1, 3] — a closed interval

The **Values** parameter

```
{Sldv.Interval(0, 1, '['), Sldv.Point(1)}
```

specifies:

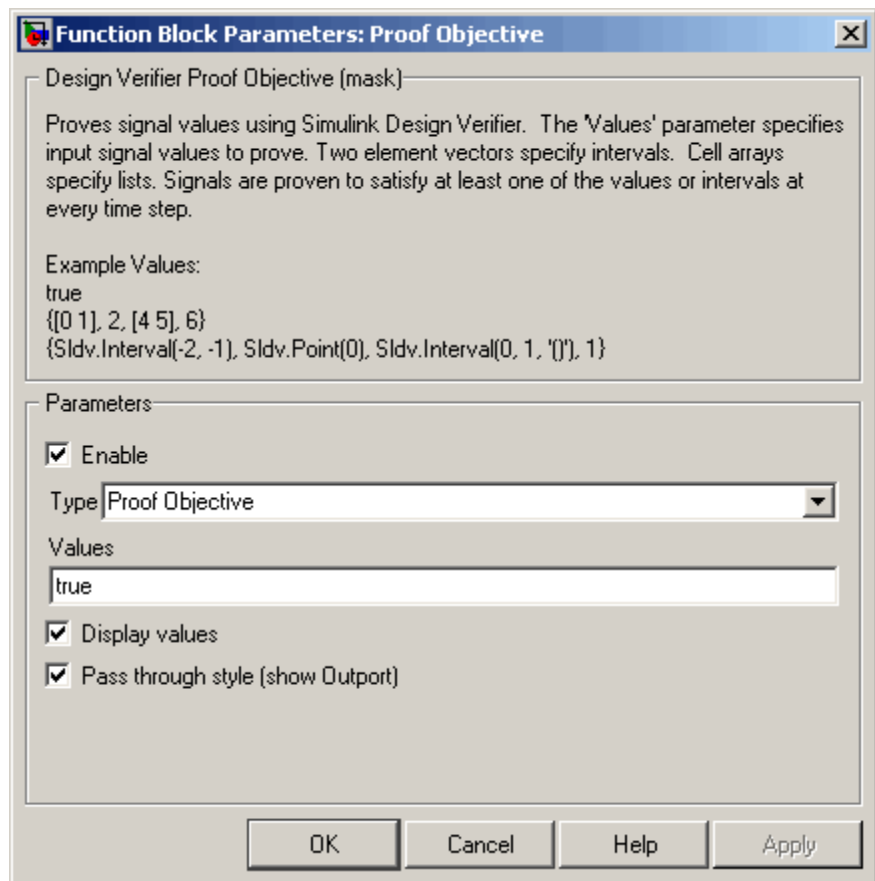
- `Sldv.Interval(0, 1, '[')` — the right-open interval [0, 1)
- `Sldv.Point(1)` — a scalar

If you specify multiple scalars and intervals for a Proof Objective block, the Simulink Design Verifier software combines them using a logical OR operation during the property proof. In this case, the software considers the entire proof objective to be satisfied if any single scalar or interval is satisfied.

Data Type Support

The Proof Objective block accepts signals of all built-in data types supported by the Simulink software. For a discussion on the data types supported by the Simulink software, see “Data Types Supported by Simulink” in *Simulink User’s Guide*.

Parameters and Dialog Box



Enable

Specify whether the block is enabled. If selected (the default), the Simulink Design Verifier software uses the block when proving properties of a model. Clearing this option disables the block, that is, causes the Simulink Design Verifier software to behave as if the Proof Objective block did not exist. If this option is not selected, the block appears grayed out in the model editor.

Proof Objective

Type

Specify whether the block behaves as a Proof Objective or Test Objective block. Select **Test Objective** to transform the Proof Objective block into a Test Objective block.

Values

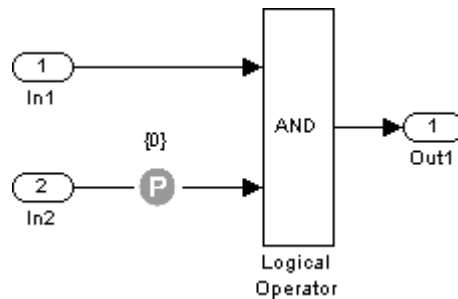
Specify the proof objective (see “Specifying Proof Objectives” on page 12-8).

Display values

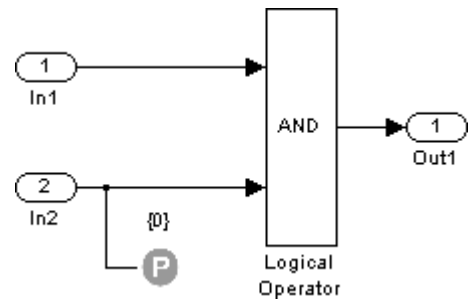
Specify whether the block displays the contents of its **Values** parameter in the model editor. By default, this option is selected.

Pass through style

Specify whether the block displays an output port in the model editor. If selected (the default), the block displays its output port, allowing its input signal to pass through as the block output. If not selected, the block hides its output port and terminates the input signal. The following figure illustrates the appearance of the block in each case.



Pass through style: selected



Pass through style: deselected

See Also

Proof Assumption, Test Objective

Purpose

Constrain signal values in test cases

Library

Simulink Design Verifier

Description



When operating in test generation mode, the Simulink Design Verifier software produces test cases that satisfy specified criteria (see Chapter 7, “Generating Test Cases”). In this mode, you can use Test Condition blocks to define test conditions for signals in your model. The **Values** parameter lets you specify constraints on signal values during a test case simulation. The block applies the specified **Values** parameter to its input signal, and the Simulink Design Verifier software attempts to produce test cases that satisfy the condition.

The block’s parameter dialog box also allows you to

- Enable or disable the condition.
- Specify that the block should display its **Values** parameter in the model editor.
- Specify that the block should display its output port.

Note The Simulink and Real-Time Workshop software ignore the Test Condition block during model simulation and code generation, respectively. The Simulink Design Verifier software uses the Test Condition block only when generating test cases for a model.

Specifying Test Conditions

Use the **Values** parameter to constrain signal values in test cases. Specify any combination of scalars and intervals in the form of a MATLAB cell array. (For information about cell arrays, see “Cell Arrays” in the MATLAB documentation.)

Test Condition

Tip If the **Values** parameter specifies only one scalar value, you do not need to enter it in the form of a MATLAB cell array.

Scalar values each comprise a single cell in the array, for example:

`{0, 5}`

A closed interval comprises a two-element vector as a cell in the array, where each element specifies an interval endpoint:

`{[1, 2]}`

Alternatively, you can specify scalar values using the `Sldv.Point` constructor, which accepts a single value as its argument. You can specify intervals using the `Sldv.Interval` constructor, which requires two input arguments, i.e., a lower bound and an upper bound for the interval. Optionally, you can provide one of the following strings as a third input argument that specifies inclusion or exclusion of the interval endpoints:

- `'()'` — Defines an open interval.
- `'[]'` — Defines a closed interval.
- `'(]'` — Defines a left-open interval.
- `'][)'` — Defines a right-open interval.

Note By default, `Sldv.Interval` considers an interval to be closed if you omit its third input argument.

As an example, the **Values** parameter

`{0, [1, 3]}`

specifies:

- 0 — a scalar
- [1, 3] — a closed interval

The **Values** parameter

```
{Sldv.Interval(0, 1, '[') }, Sldv.Point(1)}
```

specifies:

- `Sldv.Interval(0, 1, '[')` — the right-open interval [0, 1)
- `Sldv.Point(1)` — a scalar

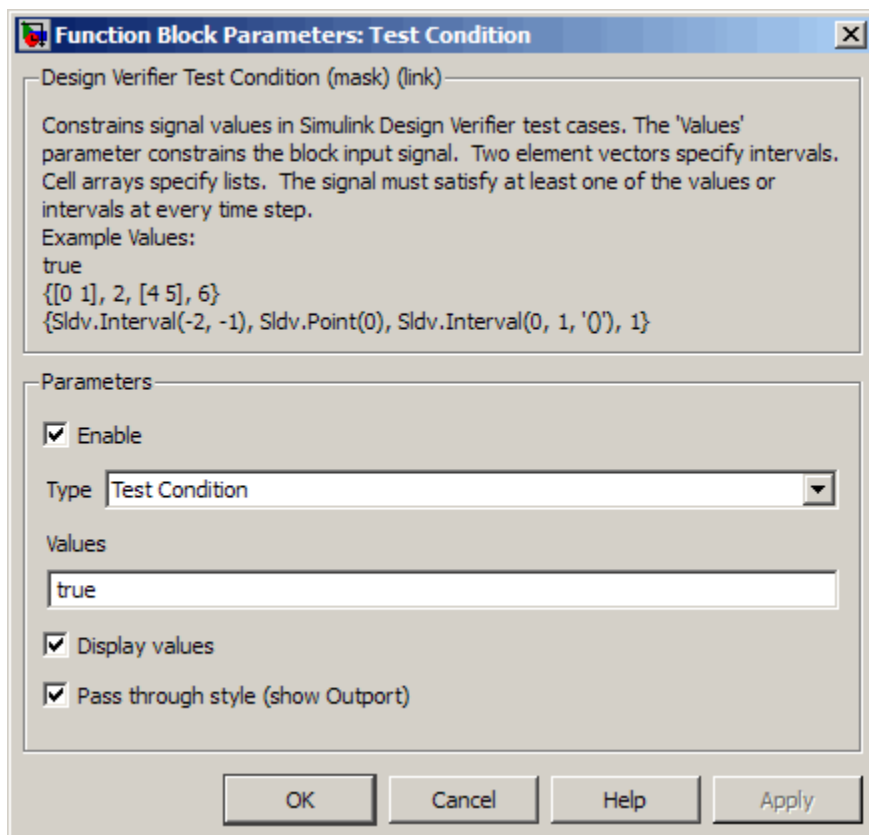
If you specify multiple scalars and intervals for a Test Condition block, the Simulink Design Verifier software combines them using a logical OR operation when generating test cases. Consequently, the software considers the entire test condition to be satisfied if any single scalar or interval is satisfied.

Data Type Support

The Test Condition block accepts signals of all built-in data types supported by the Simulink software. For a discussion on the data types supported by the Simulink software, see “Data Types Supported by Simulink” in *Simulink User’s Guide*.

Test Condition

Parameters and Dialog Box



Enable

Specify whether the block is enabled. If selected (the default), Simulink Design Verifier software uses the block when generating tests for a model. Clearing this option disables the block, that is, causes the Simulink Design Verifier software to behave as if the Test Condition block did not exist. If this option is not selected, the block appears grayed out in the model editor.

Type

Specify whether the block behaves as a Test Condition or Proof Assumption block. Select Assumption to transform the Test Condition block into a Proof Assumption block.

Values

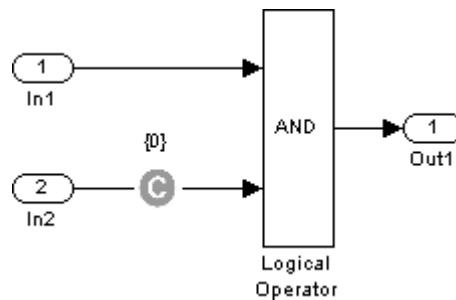
Specify the test condition (see “Specifying Test Conditions” on page 12-13).

Display values

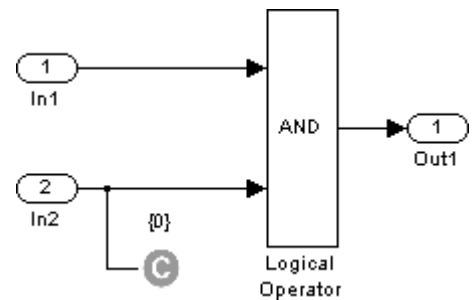
Specify whether the block displays the contents of its **Values** parameter in the model editor. By default, this option is selected.

Pass through style

Specify whether the block displays an output port in the model editor. If selected (the default), the block displays its output port, allowing its input signal to pass through as the block output. If not selected, the block hides its output port and terminates the input signal. The following figure illustrates the appearance of the block in each case.



Pass through style: selected



Pass through style: deselected

See Also

Proof Assumption, Test Objective

Test Objective

Purpose Define custom objectives that signals must satisfy in test cases

Library Simulink Design Verifier

Description



When operating in test generation mode, the Simulink Design Verifier software produces test cases that satisfy specified criteria (see Chapter 7, “Generating Test Cases”). In this mode, you can use Test Objective blocks to define custom test objectives for signals in your model. The **Values** parameter lets you specify values that a signal must achieve for at least one time step during a test case simulation. The block applies the specified **Values** parameter to its input signal, and the Simulink Design Verifier software attempts to produce test cases that satisfy the objective.

The block’s parameter dialog box also allows you to

- Enable or disable the objective.
- Specify that the block should display its **Values** parameter in the model editor.
- Specify that the block should display its output port.

Note The Simulink and Real-Time Workshop software ignore the Test Objective block during model simulation and code generation, respectively. The Simulink Design Verifier software uses the Test Objective block only when generating test cases for a model.

Specifying Test Objectives

Use the **Values** parameter to define custom objectives that signals must satisfy in test cases. Specify any combination of scalars and intervals in the form of a MATLAB cell array. (For information about cell arrays, see “Cell Arrays” in the MATLAB documentation.)

Tip If the **Values** parameter specifies only one scalar value, you do not need to enter it in the form of a MATLAB cell array.

Scalar values each comprise a single cell in the array, for example:

```
{0, 5}
```

A closed interval comprises a two-element vector as a cell in the array, where each element specifies an interval endpoint:

```
{[1, 2]}
```

Alternatively, you can specify scalar values using the `Sldv.Point` constructor, which accepts a single value as its argument. You can specify intervals using the `Sldv.Interval` constructor, which requires two input arguments, i.e., a lower bound and an upper bound for the interval. Optionally, you can provide one of the following strings as a third input argument that specifies inclusion or exclusion of the interval endpoints:

- '()' — Defines an open interval.
- '[' — Defines a closed interval.
- '(]' — Defines a left-open interval.
- '](' — Defines a right-open interval.

Note By default, `Sldv.Interval` considers an interval to be closed if you omit its third input argument.

As an example, the **Values** parameter

```
{0, [1, 3]}
```

specifies:

Test Objective

- 0 — a scalar
- [1, 3] — a closed interval

The **Values** parameter

```
{Sldv.Interval(0, 1, '['), Sldv.Point(1)}
```

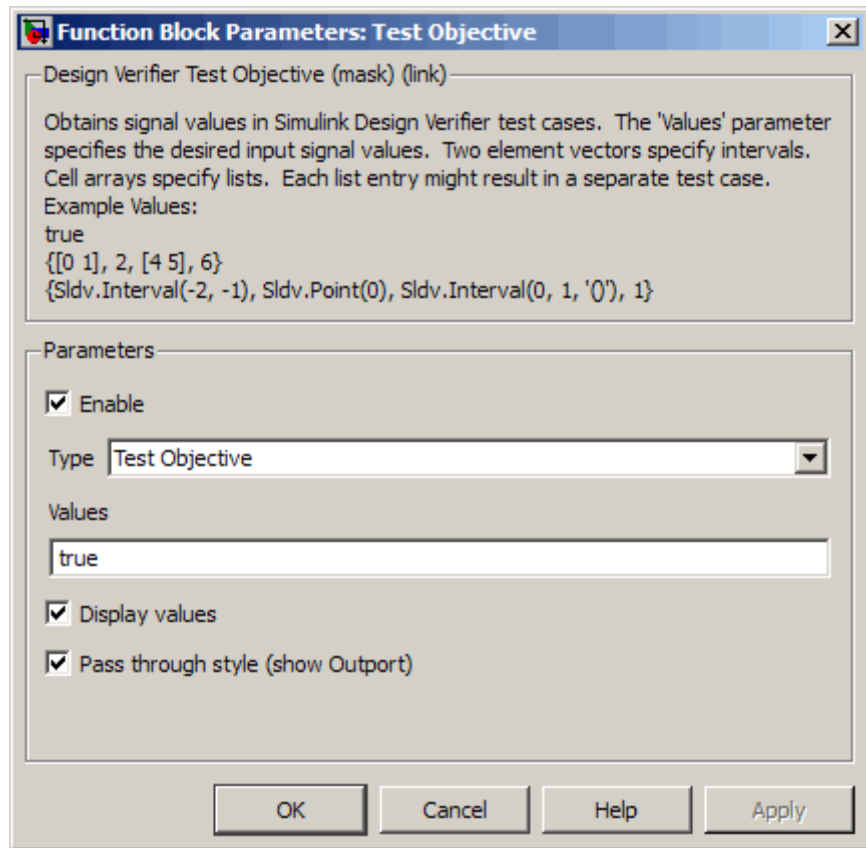
specifies:

- `Sldv.Interval(0, 1, '[')` — the right-open interval [0, 1)
- `Sldv.Point(1)` — a scalar

Data Type Support

The Test Objective block accepts signals of all built-in data types supported by the Simulink software. For a discussion on the data types supported by the Simulink software, see “Data Types Supported by Simulink” in *Simulink User’s Guide*.

Parameters and Dialog Box



Enable

Specify whether the block is enabled. If selected (the default), the Simulink Design Verifier software uses the block when generating tests for a model. Clearing this option disables the block, that is, causes the Simulink Design Verifier software to behave as if the Test Objective block did not exist. If this option is not selected, the block appears grayed out in the model editor.

Test Objective

Type

Specify whether the block behaves as a Test Objective or Proof Objective block. Select **Proof Objective** to transform the Test Objective block into a Proof Objective block.

Values

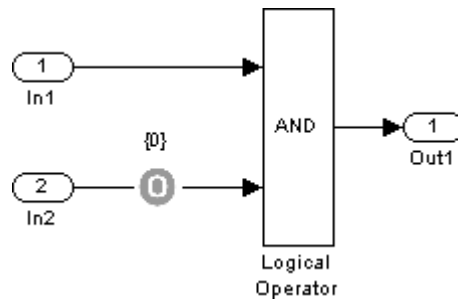
Specify the test objective (see “Specifying Test Objectives” on page 12-18).

Display values

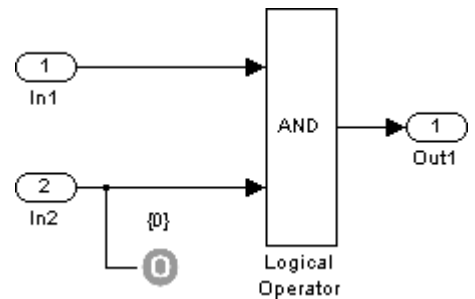
Specify whether the block displays the contents of its **Values** parameter in the model editor. By default, this option is selected.

Pass through style

Specify whether the block displays an output port in the model editor. If selected (the default), the block displays its output port, allowing its input signal to pass through as the block output. If not selected, the block hides its output port and terminates the input signal. The following figure illustrates the appearance of the block in each case.



Pass through style: selected



Pass through style: deselected

See Also

Proof Objective, Test Condition

Purpose

Represent subsystem that specifies proof or test objectives without impacting simulation results or generated code

Library

Simulink Design Verifier

Description



This block is a Subsystem block that is preconfigured to serve as a starting point for creating a subsystem that specifies proof or test objectives for use with the Simulink Design Verifier software. The Real-Time Workshop software ignores Verification Subsystem blocks during code generation, behaving as if the subsystems do not exist. A Verification Subsystem block allows you to add Simulink Design Verifier components to a model without affecting its generated code.

To create a Verification Subsystem in your model:

- 1** Copy the Verification Subsystem block from the Simulink Design Verifier library into your model.
- 2** Open the Verification Subsystem block by double-clicking it.
- 3** In the Verification Subsystem window, add blocks that specify proof or test objectives. Use Inport blocks to represent input from outside the subsystem.

The Verification Subsystem block in the Simulink Design Verifier library is preconfigured to work correctly. For correct behavior, a Verification Subsystem block must

- Contain no Output blocks.
- Enable its **Treat as Atomic Unit** parameter.
- Specify its **Mask type** parameter as `VerificationSubsystem`.

Verification Subsystem

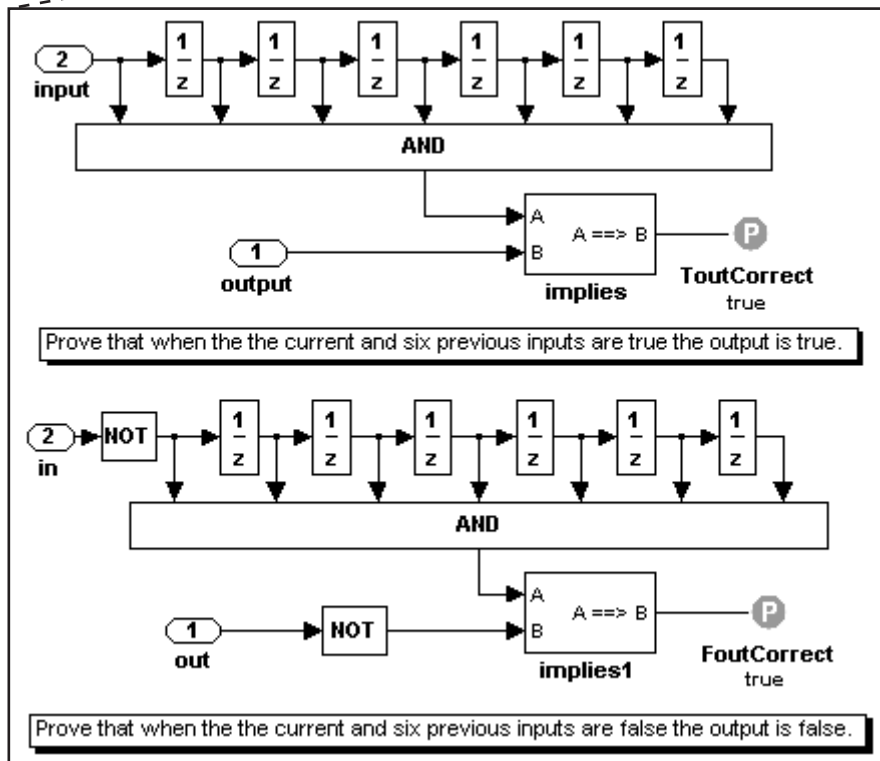
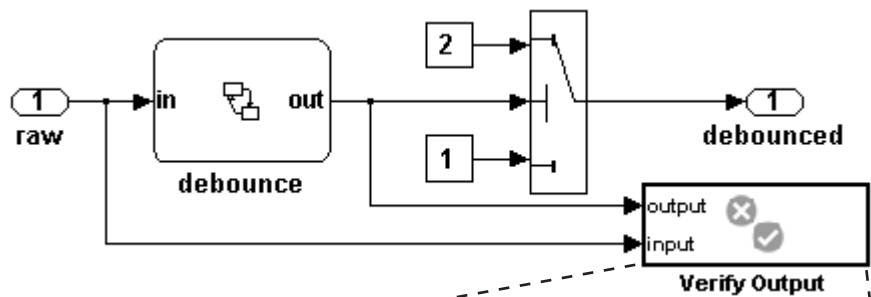
Note If you alter a Verification Subsystem block so that it no longer behaves correctly, the Simulink Design Verifier software displays a warning.

See the Subsystem block in the *Simulink Reference* and “Creating Subsystems” in *Simulink User’s Guide* for more information.

Examples

The `sldvdemo_debounce_validprop` demo model includes a Verification Subsystem that specifies two proof objectives, as shown in the following figure.

Verification Subsystem



Verification Subsystem

See Also

Proof Assumption, Proof Objective, Test Condition, Test Objective

Configuration Parameters

- “Design Verifier Pane” on page 13-2
- “Design Verifier Pane: Block Replacements” on page 13-10
- “Design Verifier Pane: Parameters” on page 13-15
- “Design Verifier Pane: Test Generation” on page 13-18
- “Design Verifier Pane: Property Proving” on page 13-26
- “Design Verifier Pane: Results” on page 13-32
- “Design Verifier Pane: Report” on page 13-46
- “Parameter Command-Line Information Summary” on page 13-52

Design Verifier Pane

The image shows a configuration window titled "Design Verifier Pane" with two main sections: "Analysis options" and "Output".

Analysis options:

- Mode: A dropdown menu set to "Test generation".
- Maximum analysis time (s): A text input field containing "600".
- Display unsatisfiable test objectives
- Automatic stubbing of unsupported blocks and functions

Output:

- Output directory: A text input field containing "sldv_output/\$ModelName\$".
- Make output file names unique by adding a suffix

In this section...

“Design Verifier Pane Overview” on page 13-3

“Mode” on page 13-3

“Maximum analysis time” on page 13-5

“Display unsatisfiable test objectives” on page 13-6

“Automatic stubbing of unsupported blocks and functions” on page 13-7

“Output directory” on page 13-8

“Make output file names unique by adding a suffix” on page 13-9

Design Verifier Pane Overview

Specify analysis options and configure Simulink Design Verifier output.

Mode

Specify whether the Simulink Design Verifier software generates test cases or proves properties.

Settings

Default: Test generation

Test generation

Generates test cases for a model.

Property proving

Proves properties of a model.

Tip

The Simulink Design Verifier software specifies the value of this option automatically if you start an analysis by selecting from the **Tools** menu either **Design Verifier > Generate Tests** or **Design Verifier > Prove Properties**.

Dependency

Selecting Test generation enables the **Display unsatisfiable test objectives** parameter.

The **Generate Tests** button changes to **Prove Properties** if the **Mode** parameter changes from Test generation to Property proving.

Command-Line Information

Parameter: DVMode

Type: string

Value: 'TestGeneration' | 'PropertyProving'

Default: 'TestGeneration'

See Also

- Generating Test Cases
- Proving Properties of a Model

Maximum analysis time

Specify the maximum time (in seconds) that the Simulink Design Verifier software spends analyzing a model.

Settings

Default: 600

The value you enter represents the maximum number of seconds the Simulink Design Verifier software analyzes your model.

Command-Line Information

Parameter: DVMaxProcessTime

Type: double

Value: any valid value

Default: 600

Display unsatisfiable test objectives

Specify whether to display a warning for unsatisfiable test objectives. For more information about using this option, see “Display unsatisfiable test objectives” on page 6-6.

Settings

Default: On



On

Displays a warning in the Simulation Diagnostics Viewer when the Simulink Design Verifier software is unable to satisfy a test objective.



Off

Does not display a warning when the Simulink Design Verifier software is unable to satisfy a test objective.

Command-Line Information

Parameter: `DVDisplayUnsatisfiableObjectives`

Type: string

Value: 'on' | 'off'

Default: 'on'

Automatic stubbing of unsupported blocks and functions

Specify whether or not Simulink Design Verifier software should ignore unsupported blocks and functions and proceed with the analysis.

Settings

Default: Off

- On
Ignores unsupported blocks and functions and proceeds with the analysis.
- Off
Displays a warning when the Simulink Design Verifier software encounters an unsupported block or function and asks if you want to continue the analysis.

Command-Line Information

Parameter: AutomaticStubbing

Type: string

Value: 'on' | 'off'

Default: 'off'

Output directory

Specify a directory to which the Simulink Design Verifier software writes its output.

Settings

Default: `sldv_output/$ModelName$`

- Enter a path that is either absolute or relative to the current directory.
- `$ModelName$` is a token that represents the model name.

Tip

You can use the following parameters to customize the names and locations of Simulink Design Verifier output:

- **Data file name**
- **Harness model file name**
- **SystemTest file name**
- **Report file name**
- **File path of the output model**

Command-Line Information

Parameter: `DVOutputDir`

Type: `string`

Value: any valid path

Default: `'sldv_output/$ModelName$'`

Make output file names unique by adding a suffix

Specify whether the Simulink Design Verifier software makes its output file names unique by appending a numeric suffix.

Settings

Default: On



On

Appends an incremental numeric suffix to Simulink Design Verifier output file names. Selecting this option prevents the software from overwriting existing files that have the same name.



Off

Does not append a suffix to Simulink Design Verifier output file names. In this case, the software might overwrite existing files that have the same name.

Command-Line Information

Parameter: DVMakeOutputFilesUnique

Type: string

Value: 'on' | 'off'

Default: 'on'

Design Verifier Pane: Block Replacements

The image shows a configuration window titled "Block replacements". It contains a checkbox labeled "Apply block replacements" which is currently unchecked. Below the checkbox is a large empty rectangular area labeled "List of block replacement rules (in order of priority):". At the bottom of the window, there is a section titled "Output model" containing a text input field labeled "File path of the output model:".

In this section...

“Block Replacements Pane Overview” on page 13-11

“Apply block replacements” on page 13-12

“List of block replacement rules” on page 13-13

“File path of the output model” on page 13-14

Block Replacements Pane Overview

Specify options that control how the Simulink Design Verifier software preprocesses the models it analyzes.

See Also

[Working with Block Replacements](#)

Apply block replacements

Specify whether the Simulink Design Verifier software replaces blocks in a model before its analysis.

Settings

Default: Off



On

Replaces blocks in a model before the Simulink Design Verifier software analyzes it.



Off

Does not replace blocks in a model before the Simulink Design Verifier software analyzes it.

Dependencies

This parameter enables **List of block replacement rules** and **File path of the output model**.

Command-Line Information

Parameter: DVBlockReplacement

Type: string

Value: 'on' | 'off'

Default: 'off'

See Also

Working with Block Replacements

List of block replacement rules

Specify a list of block replacement rules that the Simulink Design Verifier software executes before its analysis.

Settings

Default: <FactoryDefaultRules>

- Specify block replacement rules as a list delimited by spaces, commas, or carriage returns.
- The Simulink Design Verifier software processes block replacement rules in the order that you list them.
- If you specify the default value, the Simulink Design Verifier software uses its factory default block replacement rules.

Dependency

This parameter is enabled by **Apply block replacements**.

Command-Line Information

Parameter: DVBlockReplacementRulesList

Type: string

Value: any rules

Default: '<FactoryDefaultRules>'

See Also

Working with Block Replacements

File path of the output model

Specify a directory and file name for the model that results after applying block replacement rules.

Settings

Default: \$ModelName\$_replacement

- Optionally, enter a path that is either absolute or relative to the path specified in **Output directory**.
- Enter a file name for the model that results after applying block replacement rules.
- \$ModelName\$ is a token that represents the model name.

Dependency

This parameter is enabled by **Apply block replacements**.

Command-Line Information

Parameter: DVBlockReplacementModelFileName

Type: string

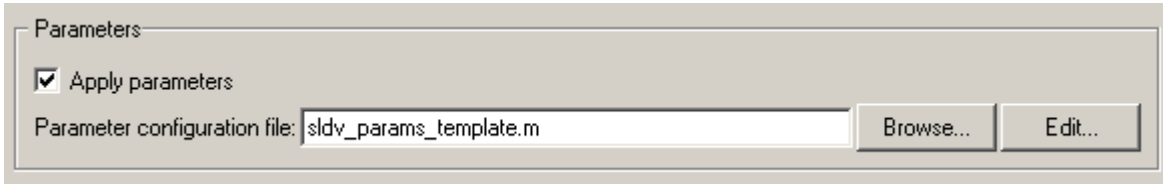
Value: any valid path and file name

Default: '\$ModelName\$_replacement'

See Also

Working with Block Replacements

Design Verifier Pane: Parameters



The image shows a screenshot of a software dialog box titled "Parameters". Inside the dialog, there is a checked checkbox labeled "Apply parameters". Below this, there is a text field labeled "Parameter configuration file:" containing the text "sldv_params_template.m". To the right of the text field are two buttons: "Browse..." and "Edit...".

In this section...

“Parameters Pane Overview” on page 13-16

“Apply parameters” on page 13-16

“Parameter configuration file” on page 13-16

Parameters Pane Overview

Specify options that control how the Simulink Design Verifier software uses parameter configurations when analyzing models.

Apply parameters

Specify whether the Simulink Design Verifier software uses parameter configurations when analyzing a model.

Settings

Default: On



On

The Simulink Design Verifier software uses parameter configurations when analyzing a model.



Off

The Simulink Design Verifier software does not use parameter configurations when analyzing a model.

Dependency

This parameter enables **Parameter configuration file**.

Command-Line Information

Parameter: DVParameters

Type: string

Value: 'on' | 'off'

Default: 'on'

See Also

Specifying Parameter Configurations

Parameter configuration file

Specify an M-file function that defines parameter configurations for a model.

Settings

Default: sldv_params_template.m

- The default file, `sldv_params_template.m`, is a template that you can edit and save. The comments in the template explain the syntax you use to specify parameter configurations.
- Click the **Browse** button to select an existing M-file function using a file chooser dialog box.
- Click the **Edit** button to open the specified M-file function in an editor.

Dependency

This parameter is enabled by **Apply parameters**.

Command-Line Information

Parameter: DVParametersConfigFileName

Type: string

Value: any valid M-file function

Default: 'sldv_params_template.m'

See Also

Specifying Parameter Configurations

Design Verifier Pane: Test Generation

The image shows a configuration window titled "Test generation" with five rows of settings:

- Model coverage objectives: MCDC
- Test conditions: Enable all
- Test objectives: Enable all
- Maximum test case steps: 500
- Test suite optimization: Combined objectives

In this section...

“Test Generation Pane Overview” on page 13-19

“Model coverage objectives” on page 13-20

“Test conditions” on page 13-21

“Test objectives” on page 13-22

“Maximum test case steps” on page 13-23

“Test suite optimization” on page 13-24

Test Generation Pane Overview

Specify options that control how the Simulink Design Verifier software generates tests for the models it analyzes.

See Also

Generating Test Cases

Model coverage objectives

Specify the type of model coverage that the Simulink Design Verifier software attempts to achieve.

Settings

Default: MCDC

None

Generates test cases that achieve only the custom objectives that you specified in your model using, for example, Test Objective blocks.

Decision

Generates test cases that achieve decision coverage.

Condition Decision

Generates test cases that achieve condition and decision coverage.

MCDC

Generates test cases that achieve modified condition/decision coverage (MCDC).

When you set **Model coverage objectives** to MCDC, the Simulink Design Verifier software automatically enables every coverage objective for decision coverage and condition coverage as well. Similarly, enabling coverage for condition coverage causes every decision and condition coverage outcome to be enabled.

Command-Line Information

Parameter: DVModelCoverageObjectives

Type: string

Value: 'None' | 'Decision' | 'ConditionDecision' | 'MCDC'

Default: 'MCDC'

See Also

Generating Test Cases

Test conditions

Specify whether Test Condition blocks in your model are enabled or disabled.

Settings

Default: Use local settings

Use local settings

Enables or disables Test Condition blocks based on the value of the **Enable** parameter of each block. If a block's **Enable** parameter is selected, the block is enabled; otherwise, the block is disabled.

Enable all

Enables all Test Condition blocks in the model regardless of the settings of their **Enable** parameters.

Disable all

Disables all Test Condition blocks in the model regardless of the settings of their **Enable** parameters.

Command-Line Information

Parameter: DVTestConditions

Type: string

Value: 'UseLocalSettings' | 'EnableAll' | 'DisableAll'

Default: 'UseLocalSettings'

See Also

- Test Condition
- Generating Test Cases

Test objectives

Specify whether Test Objective blocks in your model are enabled or disabled.

Settings

Default: Use local settings

Use local settings

Enables or disables Test Objective blocks based on the value of the **Enable** parameter of each block. If a block's **Enable** parameter is selected, the block is enabled; otherwise, the block is disabled.

Enable all

Enables all Test Objective blocks in the model regardless of the settings of their **Enable** parameters.

Disable all

Disables all Test Objective blocks in the model regardless of the settings of their **Enable** parameters.

Command-Line Information

Parameter: DVTestObjectives

Type: string

Value: 'UseLocalSettings' | 'EnableAll' | 'DisableAll'

Default: 'UseLocalSettings'

See Also

- Test Objective
- Generating Test Cases

Maximum test case steps

Specify the maximum number of simulation steps the Simulink Design Verifier software takes when attempting to satisfy a test objective.

Settings

Default: 500

You can specify a value that represents the maximum number of simulation steps the Simulink Design Verifier software takes when attempting to satisfy a test objective.

Command-Line Information

Parameter: DVMaxTestCaseSteps

Type: int32

Value: any valid value

Default: 500

See Also

Generating Test Cases

Test suite optimization

Specify the optimization strategy to use when generating test cases.

Settings

Default: Combined objectives

Combined objectives

Minimizes the number of test cases in a suite by generating cases that address more than one test objective. Each test case tends to be long, i.e., it includes many time steps.

Individual objectives

Maximizes the number of test cases in a suite by generating cases that each address only one test objective. Each test case tends to be short, i.e., it includes only a few time steps.

Large model

Minimizes the number of test cases in a suite by generating cases that address more than one test objective. This strategy is tailored for large, complex models; consequently, it tends to use all the time that the **Maximum analysis time** option allots.

Long test cases

Combines test cases to create a smaller number of test cases. This strategy generates fewer, but longer, test cases that each satisfy multiple test objectives and creates a more efficient analysis and easier-to-review results.

Tip

If an analysis using the **Combined objectives** strategy returns objectives without an outcome, set this option to **Individual objectives** and reanalyze the model. The **Individual objectives** strategy analyzes each objective independently and is better at identifying unsatisfiable objectives.

However, set this option to **Large model** if the model has both of the following characteristics:

- Nonlinearities, such as those that result from multiplying or dividing the model's input signals

- Numerous test objectives, such as those that result when using blocks that receive model coverage

The `Large model` strategy performs an analysis that is tailored to large, complex models; but, this strategy tends to use all the time that the **Maximum analysis time** option allots.

If you have a large number of test objectives, select `Long test cases` for a more efficient analysis and an easy-to-review report.

Command-Line Information

Parameter: `DVTestSuiteOptimization`

Type: `string`

Value: `'CombinedObjectives' | 'IndividualObjectives' | 'LargeModel' | 'LongTestCases'`

Default: `'CombinedObjectives'`

See Also

Generating Test Cases

Design Verifier Pane: Property Proving

Property proving

Assertion blocks:	Enable all	▼
Proof assumptions:	Enable all	▼
Strategy:	Find violation	▼
Maximum violation steps:	20	

In this section...

“Property Proving Pane Overview” on page 13-27

“Assertion blocks” on page 13-28

“Proof assumptions” on page 13-29

“Strategy” on page 13-30

“Maximum violation steps” on page 13-31

Property Proving Pane Overview

Specify options that control how the Simulink Design Verifier software proves properties for the models it analyzes.

See Also

Proving Properties of a Model

Assertion blocks

Specify whether Assertion blocks in your model are enabled or disabled.

Settings

Default: Use local settings

Use local settings

Enables or disables Assertion blocks based on the value of the **Enable** parameter of each block. If a block's **Enable** parameter is selected, the block is enabled; otherwise, the block is disabled.

Enable all

Enables all Assertion blocks in the model regardless of the settings of their **Enable** parameters.

Disable all

Disables all Assertion blocks in the model regardless of the settings of their **Enable** parameters.

Command-Line Information

Parameter: DVAssertions

Type: string

Value: 'UseLocalSettings' | 'EnableAll' | 'DisableAll'

Default: 'UseLocalSettings'

See Also

- Assertion
- Proving Properties of a Model

Proof assumptions

Specify whether Proof Assumption blocks in your model are enabled or disabled.

Settings

Default: Use local settings

Use local settings

Enables or disables Proof Assumption blocks based on the value of the **Enable** parameter of each block. If a block's **Enable** parameter is selected, the block is enabled; otherwise, the block is disabled.

Enable all

Enables all Proof Assumption blocks in the model regardless of the settings of their **Enable** parameters.

Disable all

Disables all Proof Assumption blocks in the model regardless of the settings of their **Enable** parameters.

Command-Line Information

Parameter: DVProofAssumptions

Type: string

Value: 'UseLocalSettings' | 'EnableAll' | 'DisableAll'

Default: 'UseLocalSettings'

See Also

- Proof Assumption
- Proving Properties of a Model

Strategy

Specify the strategy that the Simulink Design Verifier software uses when proving properties.

Settings

Default: Prove

Prove

Performs property proofs.

Find violation

Searches for property violations within the number of simulation steps specified by the **Maximum violation steps** option.

Prove with violation detection

Searches for property violations within the number of simulation steps specified by the **Maximum violation steps** option; then it attempts to prove properties for which it failed to detect a violation.

Dependency

Selecting Find violation or Prove with violation detection enables the **Maximum violation steps** parameter.

Command-Line Information

Parameter: DVProvingStrategy

Type: string

Value: 'Prove' | 'FindViolation' | 'ProveWithViolationDetection'

Default: 'Prove'

See Also

Proving Properties of a Model

Maximum violation steps

Specify the maximum number of simulation steps over which the Simulink Design Verifier software searches for property violations.

Settings

Default: 20

The Simulink Design Verifier software does not search beyond the maximum number of simulation steps that you specify. Therefore, it cannot identify violations that might occur later in a simulation.

Dependency

This parameter is enabled by **Strategy**.

Command-Line Information

Parameter: DVMaxViolationSteps

Type: int32

Value: any valid value

Default: 20

See Also

Proving Properties of a Model

Design Verifier Pane: Results

Data file options

Save test data to file

Data file name:

Include expected output values

Randomize data that do not affect the outcome

Harness model options

Save test harness as model

Harness model file name:

Reference input model in generated harness

SystemTest options

Save test harness as SystemTest TEST-file (will reference saved data file)

SystemTest file name:

In this section...

- “Results Pane Overview” on page 13-34
- “Save test data to file” on page 13-35
- “Data file name” on page 13-36
- “Include expected output values” on page 13-37
- “Randomize data that does not affect outcome” on page 13-39
- “Save test harness as model” on page 13-41
- “Harness model file name” on page 13-42
- “Reference input model in generated harness” on page 13-43

In this section...

“Save test harness as SystemTest TEST-file (will reference saved data file)”
on page 13-44

“SystemTest file name” on page 13-45

Results Pane Overview

Specify options that control how the Simulink Design Verifier software handles the results that it generates.

See Also

Reviewing the Results

Save test data to file

Save the test data that the Simulink Design Verifier software generates to a MAT-file.

Settings

Default: On



On

Saves the test data that the Simulink Design Verifier software generates to a MAT-file.



Off

Does not save the test data that the Simulink Design Verifier software generates.

Dependency

This parameter enables **Data file name**.

Command-Line Information

Parameter: DVSaveDataFile

Type: string

Value: 'on' | 'off'

Default: 'on'

See Also

Reviewing the Results

Data file name

Specify a directory and file name for the MAT-file that contains the data generated during the analysis, stored in an `sldvData` structure.

Settings

Default: `$ModelName$_sldvdata`

- Optionally, enter a path that is either absolute or relative to the path specified in **Output directory**.
- Enter a file name for the MAT-file.
- `$ModelName$` is a token that represents the model name.

Dependency

This parameter is enabled by **Save test data to file**.

Command-Line Information

Parameter: `DVDataFileName`

Type: string

Value: any valid path and file name

Default: `'$ModelName$_sldvdata'`

See Also

Reviewing the Results

Include expected output values

Simulate the model using test case signals and include the output values in the Simulink Design Verifier data file.

Settings

Default: Off



On

Simulates the model using the test case signals that the Simulink Design Verifier software produces. For each test case, the software collects the simulation output values associated with Outport blocks in the top-level system and includes those values in the MAT-file that it generates.



Off

Does not simulate the model and collect output values for inclusion in the MAT-file that the Simulink Design Verifier software generates.

Tips

- The `TestCases.expectedOutput` subfield of the MAT-file contains the output values. For more information, see “Anatomy of the `sldvData` Structure”.
- When **Include expected output values** is enabled, the Simulink Design Verifier software successively simulates the model using each test case that it generates. Enabling this option requires more time for the Simulink Design Verifier software to complete its analysis.

Dependency

This parameter is enabled by **Save test data to file**.

Command-Line Information

Parameter: DVSaveExpectedOutput

Type: string

Value: 'on' | 'off'

Default: 'off'

See Also

Reviewing the Results

Randomize data that does not affect outcome

Use random values instead of zeros for input signals that have no impact on test or proof objectives.

Settings

Default: Off



On

Assigns random values to test case or counterexample signals that do not affect the outcome of test or proof objectives in a model. This option can enhance traceability and improve your regression tests.

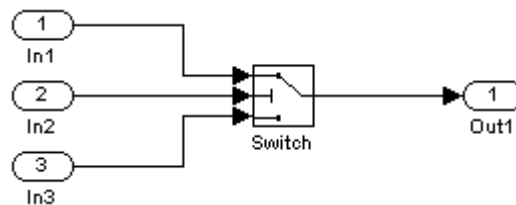


Off

Assigns zeros to test case or counterexample signals that do not affect the outcome of test or proof objectives in a model.

Tips

- This option assigns random values to test case or counterexample signals that otherwise would be zero. In the Simulink Design Verifier report, the Generated Input Data table always displays a dash (–) for such signals.
- Enable this option to enhance traceability when simulating test cases or counterexamples. For instance, consider the following model:



Only the signal entering the Switch block's control port impacts its decision coverage. If the **Randomize data that does not affect outcome** parameter is off, the Simulink Design Verifier software uses zeros to represent the signals from In1 and In3. When inspecting the results from test case or counterexample simulations, it is unclear which of these signals passes through the Switch block because they have the same value. But if the **Randomize data that does not affect outcome** parameter is on, the

software uses unique values to represent each of those signals. In this case, it is easier to determine which signal passes through the Switch block.

Dependency

This parameter is enabled by **Save test data to file**.

Command-Line Information

Parameter: DVRandomizeNoEffectData

Type: string

Value: 'on' | 'off'

Default: 'off'

See Also

Reviewing the Results

Save test harness as model

Save the test harness that the Simulink Design Verifier software generates as a model file.

Settings

Default: On



On

Saves the test harness that the Simulink Design Verifier software generates as a model file.



Off

Does not save the test harness that the Simulink Design Verifier software generates.

Dependency

This parameter enables **Harness model file name**.

Command-Line Information

Parameter: DVSaveHarnessModel

Type: string

Value: 'on' | 'off'

Default: 'on'

See Also

Reviewing the Results

Harness model file name

Specify a directory and file name for the test harness model.

Settings

Default: \$ModelName\$_harness

- Optionally, enter a path that is either absolute or relative to the path specified in **Output directory**.
- Enter a file name for the test harness model.
- \$ModelName\$ is a token that represents the model name.

Dependency

This parameter is enabled by **Save test harness as model**.

Command-Line Information

Parameter: DVHarnessModelFileName

Type: string

Value: any valid path and file name

Default: '\$ModelName\$_harness'

See Also

Reviewing the Results

Reference input model in generated harness

Use model reference to run the model in the test harness.

Settings

Default: Off

- On
Uses model reference to run the model in the test harness.
- Off
Uses a copy of the model in the test harness.

Command-Line Information

Parameter: DVModelReferenceHarness

Type: string

Value: 'on' | 'off'

Default: 'off'

See Also

Reviewing the Results

Save test harness as SystemTest TEST-file (will reference saved data file)

Save the test harness as a SystemTest TEST-file so you can run test cases using the SystemTest capabilities.

Note The option to create a SystemTest TEST-file is only available in test-generation mode; you cannot create this file when running a property-proving analysis.

Settings

Default: Off



On

Saves the test harness as a SystemTest TEST-file.



Off

Does not save the test harness as a SystemTest TEST-file.

Dependency

This parameter enables **SystemTest file name**.

Command-Line Information

Parameter: DVSaveSystemTestHarness

Type: string

Value: 'on' | 'off'

Default: 'off'

See Also

Reviewing the Results

SystemTest file name

Specify a directory and file name for the SystemTest TEST-file.

Settings

Default: \$ModelName\$_harness

- Optionally, enter a path that is either absolute or relative to the path specified in **Output directory**.
- Enter a file name for the SystemTest TEST-file.
- \$ModelName\$ is a token that represents the model name.

Dependency

This parameter is enabled by **Save test harness as SystemTest TEST-file (will reference saved data file)**.

Command-Line Information

Parameter: DVMSystemTestFileName

Type: string

Value: any valid path and file name

Default: '\$ModelName\$_harness'

See Also

Reviewing the Results

Design Verifier Pane: Report

Report

Generate report of the results

Report file name:

Include screen shots of properties and test objectives

Display report

In this section...

“Report Pane Overview” on page 13-47

“Generate report of the results” on page 13-48

“Report file name” on page 13-49

“Include screen shots of properties and text objectives” on page 13-50

“Display report” on page 13-51

Report Pane Overview

Specify options that control how the Simulink Design Verifier software reports its results.

See Also

Reviewing the Results

Generate report of the results

Generate and save a Simulink Design Verifier report.

Settings

Default: on

- On
Saves the HTML report that the Simulink Design Verifier software generates.
- Off
Does not generate a Simulink Design Verifier report.

Dependencies

When this parameter is enabled, you must enable **Save test harness as model**.

This parameter enables the following parameters:

- **Report file name**
- **Include screen shots of properties and test objectives**
- **Display report**

Command-Line Information

Parameter: DVSaveReport

Type: string

Value: 'on' | 'off'

Default: 'on'

See Also

Reviewing the Results

Report file name

Specify a directory and file name for the report that Simulink Design Verifier software generates.

Settings

Default: \$ModelName\$_report

- Optionally, enter a path that is either absolute or relative to the path specified in **Output directory**.
- Enter a file name for the report Simulink Design Verifier software generates.
- \$ModelName\$ is a token that represents the model name.

Dependency

This parameter is enabled by **Generate report of the results**.

Command-Line Information

Parameter: DVReportFileName

Type: string

Value: any valid path and file name

Default: '\$ModelName\$_report'

See Also

Reviewing the Results

Include screen shots of properties and text objectives

Includes screen shots of properties in the Simulink Design Verifier report. Only valid in property-proving mode.

Settings

Default: Off



On

Includes screen shots of properties in the Simulink Design Verifier report. Only valid in property-proving mode.



Off

Does not include screen shots of properties in the Simulink Design Verifier report.

Dependency

This parameter is enabled by **Generate report of the results**.

Command-Line Information

Parameter: DVReportIncludeGraphics

Type: string

Value: 'on' | 'off'

Default: 'off'

See Also

Reviewing the Results

Display report

Display the report that the Simulink Design Verifier software generates after completing its analysis.

Settings

Default: On



On

Displays the report that the Simulink Design Verifier software generates after completing its analysis.



Off

Does not display the report that the Simulink Design Verifier software generates after completing its analysis.

Dependency

This parameter is enabled by **Generate report of the results**.

Command-Line Information

Parameter: DVDisplayReport

Type: string

Value: 'on' | 'off'

Default: 'on'

See Also

Reviewing the Results

Parameter Command-Line Information Summary

The following table lists parameters that you can use to configure the behavior of the Simulink Design Verifier software. Use the `get_param` and `set_param` functions to retrieve and specify values for these parameters programmatically.

For each parameter listed in the table, the **Description** column indicates where you can set its value on the Configuration Parameters dialog box. The **Values** column shows the type of value required, the possible values (separated with a vertical line), and the default value (enclosed in braces).

Parameter	Description	Values
DVAssertions	Set by the Assertion blocks option on the Design Verifier > Property Proving pane of the Configuration Parameters dialog box.	'EnableAll' 'DisableAll' {'UseLocalSettings'}
DVBlockReplacement	Set by the Apply block replacements option on the Design Verifier > Block Replacements pane of the Configuration Parameters dialog box.	'on' {'off'}
DVBlockReplacementModel-FileName	Set by the File path of the output model option on the Design Verifier > Block Replacements pane of the Configuration Parameters dialog box.	string {'\$modelName\$_replacement'}
DVBlockReplacementRules-List	Set by the List of block replacement rules option on the Design Verifier > Block Replacements pane of the Configuration Parameters dialog box.	string {'<FactoryDefaultRules>'}

Parameter	Description	Values
DVDataFileName	Set by the Data file name option on the Design Verifier > Results pane of the Configuration Parameters dialog box.	string { '\$ModelName\$_sldvdata' }
DVDisplayUnsatisfiableObjectives	Set by the Display unsatisfiable test objectives option on the Design Verifier pane of the Configuration Parameters dialog box.	{ 'on' } 'off'
DVHarnessModelFileName	Set by the Harness model file name option on the Design Verifier > Results pane of the Configuration Parameters dialog box.	string { '\$ModelName\$_harness' }
DVMakeOutputFilesUnique	Set by the Make output file names unique by adding a suffix check box on the Design Verifier pane of the Configuration Parameters dialog box.	{ 'on' } 'off'
DVMaxProcessTime	Set by the Maximum analysis time option on the Design Verifier pane of the Configuration Parameters dialog box.	double { '600' }
DVMaxTestCaseSteps	Set by the Maximum test case steps option on the Design Verifier > Test Generation pane of the Configuration Parameters dialog box.	int32 { '500' }

Parameter	Description	Values
DVMaxViolationSteps	Set by the Maximum violation steps option on the Design Verifier > Property Proving pane of the Configuration Parameters dialog box.	int32 {'20'}
DVMode	Set by the Mode option on the Design Verifier pane of the Configuration Parameters dialog box.	{'TestGeneration'} 'PropertyProving'
DVModelCoverageObjectives	Set by the Model coverage objectives option on the Design Verifier > Test Generation pane of the Configuration Parameters dialog box.	'None' 'Decision' 'ConditionDecision' {'MCDC'}
DVModelReferenceHarness	Set by the Reference input model in generated harness option on the Design Verifier > Results pane of the Configuration Parameters dialog box.	'on' {'off'}
DVOutputDir	Set by the Output directory option on the Design Verifier pane of the Configuration Parameters dialog box.	string {'sldv_output/\$ModelName\$'}
DVOutputDir	Set by the Output directory option on the Design Verifier pane of the Configuration Parameters dialog box.	string {'sldv_output/\$ModelName\$'}

Parameter	Description	Values
DVParameters	Set by the Apply parameters option on the Design Verifier > Parameters pane of the Configuration Parameters dialog box.	{'on'} {'off'}
DVParametersConfigFileName	Set by the Parameter configuration file option on the Design Verifier > Parameters pane of the Configuration Parameters dialog box.	string {'sldv_params_template.m'}
DVProofAssumptions	Set by the Proof assumptions option on the Design Verifier > Property Proving pane of the Configuration Parameters dialog box.	'EnableAll' 'DisableAll' {'UseLocalSettings'}
DVProvingStrategy	Set by the Strategy option on the Design Verifier > Property Proving pane of the Configuration Parameters dialog box.	'FindViolation' {'Prove'} 'ProveWithViolationDetection'
DVRandomizeNoEffectData	Set by the Randomize data that does not affect outcome option on the Design Verifier > Results pane of the Configuration Parameters dialog box.	'on' {'off'}
DVReportFileName	Set by the Report file name option on the Design Verifier > Report pane of the Configuration Parameters dialog box.	string {'\$ModelName\$_report'}

Parameter	Description	Values
DVReportIncludeGraphics	Set by the Include screen shots of properties and test objectives option on the Design Verifier > Report pane of the Configuration Parameters dialog box.	'on' {'off'}
DVSaveDataFile	Set by the Save test data to file option on the Design Verifier > Results pane of the Configuration Parameters dialog box.	{'on'} 'off'
DVSaveExpectedOutput	Set by the Include expected output values option on the Design Verifier > Results pane of the Configuration Parameters dialog box.	'on' {'off'}
DVSaveHarnessModel	Set by the Save test harness as model option on the Design Verifier > Results pane of the Configuration Parameters dialog box.	{'on'} 'off'
DVSaveReport	Set by the Generate report of the results option on the Design Verifier > Report pane of the Configuration Parameters dialog box.	{'on'} 'off'
DVSaveSystemTestHarness	Set by the Save text harness as SystemTest TEST-file (will reference saved data file) option on the Design Verifier > Results pane of the Configuration Parameters dialog box.	'on' {'off'}

Parameter	Description	Values
DVSystemTestFileName	Set by the SystemTest file name option on the Design Verifier > Results pane of the Configuration Parameters dialog box.	string { '\$modelName\$_harness' }
DVTestConditions	Set by the Test conditions option on the Design Verifier > Test Generation pane of the Configuration Parameters dialog box.	'EnableAll' 'DisableAll' { 'UseLocalSettings' }
DVTestObjectives	Set by the Test objectives option on the Design Verifier > Test Generation pane of the Configuration Parameters dialog box.	'EnableAll' 'DisableAll' { 'UseLocalSettings' }
DVTestSuiteOptimization	Set by the Test suite optimization option on the Design Verifier > Test Generation pane of the Configuration Parameters dialog box.	{ 'CombinedObjectives' } 'IndividualObjectives' 'LargeModel' 'LongTestCases'

Simulink Block Support

- “Overview of Simulink Block Support” on page 14-2
- “Additional Math and Discrete Library” on page 14-3
- “Commonly Used Blocks Library” on page 14-4
- “Continuous Library” on page 14-5
- “Discontinuities Library” on page 14-6
- “Discrete Library” on page 14-7
- “Logic and Bit Operations” on page 14-8
- “Lookup Tables Library” on page 14-9
- “Math Operations” on page 14-10
- “Model Verification Library” on page 14-12
- “Model-Wide Utilities Library” on page 14-13
- “Ports & Subsystems Library” on page 14-14
- “Signal Attributes Library” on page 14-15
- “Signal Routing Library” on page 14-16
- “Sinks Library” on page 14-17
- “Sources Library” on page 14-18
- “User-Defined Functions Library” on page 14-19

Overview of Simulink Block Support

The following tables summarize the Simulink Design Verifier software's support for Simulink blocks. Each table lists all the blocks in that Simulink library and support information for that particular block. A dash (—) indicates that the software supports that block under all conditions.

If the software does not support a given block, you can turn on automatic stubbing, which considers the interface of the unsupported blocks, but not their behavior. However, if any of the unsupported blocks affect the simulation outcome, the analysis may achieve only partial results.

For details about automatic stubbing, see “Handling Incompatibilities with Automatic Stubbing” on page 2-6.

Additional Math and Discrete Library

Block	Support Notes
Decrement Real World	—
Decrement Stored Integer	—
Decrement Time To Zero	—
Decrement To Zero	—
Fixed-Point State-Space	—
Increment Real World	—
Increment Stored Integer	—
Transfer Fcn Direct Form II	Not supported
Transfer Fcn Direct Form II Time Varying	Not supported
Unit Delay Enabled	—
Unit Delay Enabled External IC	—
Unit Delay Enabled Resettable	—
Unit Delay Enabled Resettable External IC	—
Unit Delay External IC	—
Unit Delay Resettable	—
Unit Delay Resettable External IC	—
Unit Delay With Preview Enabled	—
Unit Delay With Preview Enabled Resettable	—
Unit Delay With Preview Enabled Resettable External RV	—
Unit Delay With Preview Resettable	—
Unit Delay With Preview Resettable External RV	—

Commonly Used Blocks Library

The Commonly Used Blocks library includes blocks from other libraries. Those blocks are listed under their respective libraries.

Continuous Library

Block	Support Notes
Derivative	Not supported
Integrator	Not supported
State-Space	Not supported
Transfer Fcn	Not supported
Transport Delay	Not supported
Variable Time Delay	Not supported
Variable Transport Delay	Not supported
Zero-Pole	Not supported

Discontinuities Library

Block	Support Notes
Backlash	Not supported
Coulomb & Viscous Friction	—
Dead Zone	Not supported
Dead Zone Dynamic	—
Hit Crossing	—
Quantizer	—
Rate Limiter	Supports only input and output signals of data type single or double.
Rate Limiter Dynamic	—
Relay	—
Saturation	—
Saturation Dynamic	—
Wrap To Zero	—

Discrete Library

Block	Support Notes
Difference	—
Discrete Derivative	Not supported
Discrete Filter	—
Discrete FIR Filter	—
Discrete State-Space	Not supported
Discrete Transfer Fcn	Not supported
Discrete Zero-Pole	Not supported
Discrete-Time Integrator	—
First-Order Hold	—
Integer Delay	—
Memory	—
Tapped Delay	Not supported
Transfer Fcn First Order	—
Transfer Fcn Lead or Lag	—
Transfer Fcn Real Zero	—
Unit Delay	—
Zero-Order Hold	—

Logic and Bit Operations

Block	Support Notes
Bit Clear	—
Bit Set	—
Bitwise Operator	—
Combinatorial Logic	—
Compare To Constant	—
Compare To Zero	—
Detect Change	—
Detect Decrease	—
Detect Fall Negative	—
Detect Fall Nonpositive	—
Detect Increase	—
Detect Rise Nonnegative	—
Detect Rise Positive	—
Extract Bits	—
Interval Test	—
Interval Test Dynamic	—
Logical Operator	—
Relational Operator	—
Shift Arithmetic	Not supported when the Number of bits to shift right parameter specifies a vector and the block's input or output signal has a data type other than <code>single</code> or <code>double</code> .

Lookup Tables Library

Block	Support Notes
Cosine	Not supported
Direct Lookup Table (n-D)	Not supported
Interpolation Using Prelookup	Not supported
Lookup Table	Input and output must have the same data type, either single or double.
Lookup Table (2-D)	Input and output must have the same data type, either single or double.
Lookup Table (n-D)	<p>Input and output must have the same data type, either single or double.</p> <p>Not supported when either the Interpolation method or the Extrapolation method parameter specifies Cubic Spline.</p> <p>Supports only Number of table dimensions that specify either 1 or 2.</p>
Lookup Table Dynamic	Not supported
Prelookup	—
Sine	Not supported

Math Operations

Block	Support Notes								
Abs	—								
Add	—								
Algebraic Constraint	—								
Assignment	—								
Bias	—								
Complex to Magnitude-Angle	—								
Complex to Real-Imag	—								
Divide	—								
Dot Product	—								
Gain	—								
Magnitude-Angle to Complex	Not supported								
Math Function	<table border="1"> <thead> <tr> <th>These signal types...</th> <th>Support these function parameter settings</th> </tr> </thead> <tbody> <tr> <td>All</td> <td> <ul style="list-style-type: none"> • conj • mod • rem </td> </tr> <tr> <td>Floating point</td> <td> <ul style="list-style-type: none"> • magnitude^2 • square • reciprocal • transpose • hermitian </td> </tr> <tr> <td>Integer or fixed-point</td> <td> <ul style="list-style-type: none"> • sqrt </td> </tr> </tbody> </table>	These signal types...	Support these function parameter settings	All	<ul style="list-style-type: none"> • conj • mod • rem 	Floating point	<ul style="list-style-type: none"> • magnitude^2 • square • reciprocal • transpose • hermitian 	Integer or fixed-point	<ul style="list-style-type: none"> • sqrt
These signal types...	Support these function parameter settings								
All	<ul style="list-style-type: none"> • conj • mod • rem 								
Floating point	<ul style="list-style-type: none"> • magnitude^2 • square • reciprocal • transpose • hermitian 								
Integer or fixed-point	<ul style="list-style-type: none"> • sqrt 								

Block	Support Notes
Matrix Concatenate	—
MinMax	—
MinMax Running Resetable	—
Permute Dimensions	—
Polynomial	—
Product	—
Product of Elements	—
Real-Imag to Complex	Not supported
Reshape	—
Rounding Function	—
Sign	—
Sine Wave Function	Not supported
Slider Gain	—
Squeeze	—
Subtract	—
Sum	—
Sum of Elements	—
Trigonometric Function	Not supported
Unary Minus	—
Vector Concatenate	—
Weighted Sample Time Math	Not supported

Model Verification Library

The Simulink Design Verifier software supports all blocks in the Model Verification library.

Model-Wide Utilities Library

Block	Support Notes
Block Support Table	—
DocBlock	—
Model Info	—
Time-Based Linearization	Not supported
Trigger-Based Linearization	Not supported

Ports & Subsystems Library

Block	Support Notes
Atomic Subsystem	—
Code Reuse Subsystem	—
Configurable Subsystem	—
Enabled Subsystem	—
Enabled and Triggered Subsystem	Not supported when the trigger control signal specifies a fixed-point data type.
For Iterator Subsystem	—
Function-Call Generator	—
Function-Call Subsystem	—
If	Parameter configurations are not supported for the If and Fcn blocks. The Simulink Design Verifier software ignores any parameter configurations that you specify for these blocks.
If Action Subsystem	—
Model	Supported except for limitations described in “Limitations of Support for Model Reference” on page 3-10.
Subsystem	—
Switch Case	—
Switch Case Action Subsystem	—
Triggered Subsystem	Not supported when the trigger control signal specifies a fixed-point data type.
While Iterator Subsystem	—

Signal Attributes Library

Block	Support Notes
Bus to Vector	—
Data Type Conversion	—
Data Type Conversion Inherited	—
Data Type Duplicate	—
Data Type Propagation	—
Data Type Scaling Strip	—
IC	—
Probe	—
Rate Transition	—
Signal Conversion	—
Signal Specification	—
Weighted Sample Time	Not supported
Width	Not supported

Signal Routing Library

The Simulink Design Verifier software supports all blocks in the Signal Routing library.

Sinks Library

Block	Support Notes
Display	—
Floating Scope	—
Outport (Out1)	—
Scope	—
Stop Simulation	Not supported
Terminator	—
To File	—
To Workspace	—
XY Graph	—

Sources Library

Block	Support Notes
Band-Limited White Noise	Not supported
Chirp Signal	Not supported
Clock	—
Constant	—
Counter Free-Running	—
Counter Limited	—
Digital Clock	—
From File	Not supported
From Workspace	Not supported
Ground	—
Inport (In1)	—
Pulse Generator	Supports only <code>Sample</code> based for the Pulse type parameter; also, must specify a discrete sample time.
Ramp	—
Random Number	Not supported
Repeating Sequence	Not supported
Repeating Sequence Interpolated	Not supported
Repeating Sequence Stair	—
Signal Builder	Not supported
Signal Generator	Not supported
Sine Wave	Not supported
Step	—
Uniform Random Number	Not supported

User-Defined Functions Library

Block	Support Notes
Embedded MATLAB Function	For limitations, see “Support Limitations for the Embedded MATLAB Subset” on page 3-14 for more information.
Fcn	<p>Supports all operators except ^, and supports only the mathematical functions <code>abs</code>, <code>ceil</code>, <code>fabs</code>, <code>floor</code>, <code>rem</code>, and <code>sgn</code>.</p> <p>Parameter configurations are not supported for the If and Fcn blocks. The Simulink Design Verifier software ignores any parameter configurations that you specify for these blocks.</p>
Level-2 M-file S-Function	Not supported
MATLAB Fcn	Not supported
S-Function	Not supported
S-Function Builder	Not supported

Embedded MATLAB Subset Support

This table lists only the Embedded MATLAB library functions for which the Simulink Design Verifier software provides no support or limited support. See “Embedded MATLAB Function Library Reference” for the complete listing of available functions.

Function	Support Notes
Arithmetic Operator Functions	
mldivide (\)	Supports only scalar arguments.
mpower (^)	Supports only integer exponents.
mrdivide (/)	Supports only scalar arguments.
power (.^)	Supports only integer exponents.
Casting Functions	
char	Not supported.
typecast	Not supported.
Complex Number Functions	
complex	Not supported.
imag	Not supported.
Error-Handling Functions	
assert	Supported, but does not behave like a Proof Objective block.
Exponential Functions	
exp	Not supported.
expm	Not supported.
expm1	Not supported.
log	Not supported.
log2	Not supported.
log10	Not supported.
log1p	Not supported.
nextpow2	Not supported.

Function	Support Notes
nthroot	Not supported.
reallog	Not supported.
realpow	Not supported.
realsqrt	Not supported.
sqrt	Not supported.
Filtering and Convolution Functions	
detrend	Not supported.
Fixed-Point Toolbox™ Functions	
complex	Not supported.
Interpolation and Computational Geometry	
cart2pol	Not supported.
cart2sph	Not supported.
pol2cart	Not supported.
sph2cart	Not supported.
Matrix and Array Functions	
angle	Not supported.
cond	Not supported.
det	Not supported.
eig	Not supported.
inv	Not supported.
invhilb	Not supported.
logspace	Not supported.
lu	Not supported.
norm	Supported only when invoked using the syntax $\text{norm}(A,p)$ where p is either 1 or inf .

Function	Support Notes
normest	Not supported.
pinv	Not supported.
planerot	Not supported.
qr	Not supported.
rank	Not supported.
rcond	Not supported.
subspace	Not supported.
Polynomial Functions	
poly	Not supported.
polyfit	Not supported.
Signal Processing Functions	
chol	Not supported.
fft	Not supported.
fftshift	Not supported.
ifft	Not supported.
ifftshift	Not supported.
sosfilt	Not supported.
svd	Not supported.
Special Values	
rand	Not supported.
randn	Not supported.
Specialized Math	
beta	Not supported.
betainc	Not supported.
betaln	Not supported.
ellipke	Not supported.

Function	Support Notes
erf	Not supported.
erfc	Not supported.
erfcinv	Not supported.
erfcx	Not supported.
erfinv	Not supported.
expint	Not supported.
gamma	Not supported.
gammainc	Not supported.
gamma1n	Not supported.
Statistical Functions	
std	Not supported.
String Functions	
char	Not supported.
ischar	Not supported.
Trigonometric Functions	
acos	Not supported.
acosd	Not supported.
acosh	Not supported.
acot	Not supported.
acotd	Not supported.
acoth	Not supported.
acsc	Not supported.
acscd	Not supported.
acsch	Not supported.
asec	Not supported.
asecd	Not supported.

Function	Support Notes
asech	Not supported.
asin	Not supported.
asinh	Not supported.
atan	Not supported.
atan2	Not supported.
atand	Not supported.
atanh	Not supported.
cos	Not supported.
cosd	Not supported.
cosh	Not supported.
cot	Not supported.
cotd	Not supported.
coth	Not supported.
csc	Not supported.
cscd	Not supported.
csch	Not supported.
hypot	Not supported.
sec	Not supported.
secd	Not supported.
sech	Not supported.
sin	Not supported.
sind	Not supported.
sinh	Not supported.
tan	Not supported.
tand	Not supported.
tanh	Not supported.

analysis model

The target model for a Simulink Design Verifier analysis. If you select an atomic subsystem for analysis, the analysis model is generated by extracting the subsystem to a new model.

assumption

A property that is assumed to be true during a property proof. The proof result holds only when the assumption is true.

block replacement rule

A rule that is registered with the Simulink Design Verifier software and defines how instances of specific blocks are replaced by an alternate implementation. The software uses M-code to define when and how to apply a block replacement rule (see Chapter 4, “Working with Block Replacements”).

condition coverage

Measures the percentage of the total number of logic conditions associated with logical model objects that the simulation actually exercised. Enabling condition coverage causes every decision and condition coverage outcome to be enabled. See “Types of Model Coverage” in the *Simulink Verification and Validation User’s Guide*.

constraint

A property that is forced to be true during test case generation.

counterexample

A test case that demonstrates a property violation.

coverage objective

A test objective that defines when a coverage point results in a particular outcome.

coverage point

A decision, condition, or MCDC expression associated with a model object. Each coverage point has a fixed number of mutually exclusive outcomes.

decision coverage

Measures the percentage of the total number of simulation paths through model objects that the simulation actually traversed. Decision coverage is a subset of modified decision/condition coverage. See “Types of Model Coverage” in the *Simulink Verification and Validation User’s Guide*.

floating-point approximation

The process of approximating floating-point numbers using rational numbers (i.e., fractions whose numerator and denominator are small integers). The Simulink Design Verifier software performs floating-point approximations during its analysis. It can generate invalid test cases that result from numerical differences. For example, given a sufficiently large floating-point number x , the expression $x == (x+1)$ is true; however, this expression never holds if x is a rational number.

invalid test case

A test case that does not satisfy its objectives.

modified condition/decision coverage (MCDC)

Measures the independence of logical block inputs and transition conditions associated with logical model objects during the simulation. When you set the coverage objective to MCDC, Simulink Design Verifier automatically enables every coverage objective for decision coverage and condition coverage as well. See “Types of Model Coverage” in the *Simulink Verification and Validation User’s Guide*.

nonlinear arithmetic

A computation in the model that cannot be expressed as a combination of mutually exclusive linear expressions. Nonlinear arithmetic can affect a property or test objective, and it can cause the analysis to return an error. In this case, you should apply simplifying approximations and abstractions.

property

A logical expression of the signals and data values, within a model, that is intended to be proven true during simulation. Properties evaluate at specific points in the model.

property violation

The condition during a simulation when a property is false.

test case

A sequence of numeric values and input data time that you input to a model during its simulation.

test harness

A model that runs test cases on an analysis model.

test objective

A logical expression of the signals and data values, within a model, that is intended to be true at least once in the resulting test case during simulation. Test objectives evaluate at specific points in the model.

Test Objective block

The block that you add to a model to define test objectives. In the block mask, define test objectives as values or ranges that an input signal must satisfy during a test case.

unsatisfiable test objective

The status of a test objective that indicates a test case cannot be generated for the specified approximations. This includes floating-point approximations and maximum-step limitations specified in the **Test Generation** pane of the Configuration Parameters dialog box.

validated property

The status of a property that indicates no counterexample exists, subject to floating-point approximations and the settings specified in the **Property Proving** pane of the Configuration Parameters dialog box.

Examples

Use this list to find examples in the documentation.

Automatic Stubbing

“Analyzing a Model Using Automatic Stubbing” on page 2-6

Working with Block Replacements

“Specifying Replacement Blocks” on page 4-7

“Writing Block Replacement Rules” on page 4-10

“Configuring Block Replacements” on page 4-15

Specifying Parameter Configurations

“Constructing the Example Model” on page 5-8

“Parameterizing the Constant Block” on page 5-10

“Specifying a Parameter Configuration” on page 5-11

“Analyzing the Example Model” on page 5-13

“Simulating the Test Cases” on page 5-15

Generating Test Cases

“Constructing the Example Model” on page 7-5

“Checking Compatibility of the Example Model” on page 7-6

“Configuring Test Generation Options” on page 7-10

“Analyzing the Example Model” on page 7-13

“Customizing Test Generation” on page 7-21

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Proving Properties of a Model

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